

COMPAL CONFIDENTIAL

MODEL NAME : DDP80

PCB NO : LA-F711P

BOM P/N :

GPIO MAP: Dell GPIO map EC16 062416 Compal Only

Breckenridge MLK 15 UMA

Cof fee Lake H

2018-01-11

REV : 0.5 (X02)

@ : Nopop Component

EMI@ : EMI Component

@EMI@ : EMI Nopop Component

ESD@ : ESD Component

@ESD@ : ESD Nopop Component

RF@ : RF Component

@RF@ : RF Nopop Component

XDP@ : XDP Component

CONN@ : Connector Component

eSPI@ : eSPI interface

LPC@ : LPC interface

15U@ : Lat it ude conf i

15P@ : Precision conf i g

DS3@ : Deep sleep support

NDS3@ : non Deep sleep support

MB PCB

Part Number	Description
DA8001D0000	PCB 26H LA-F711P REV0 MB UMA 1

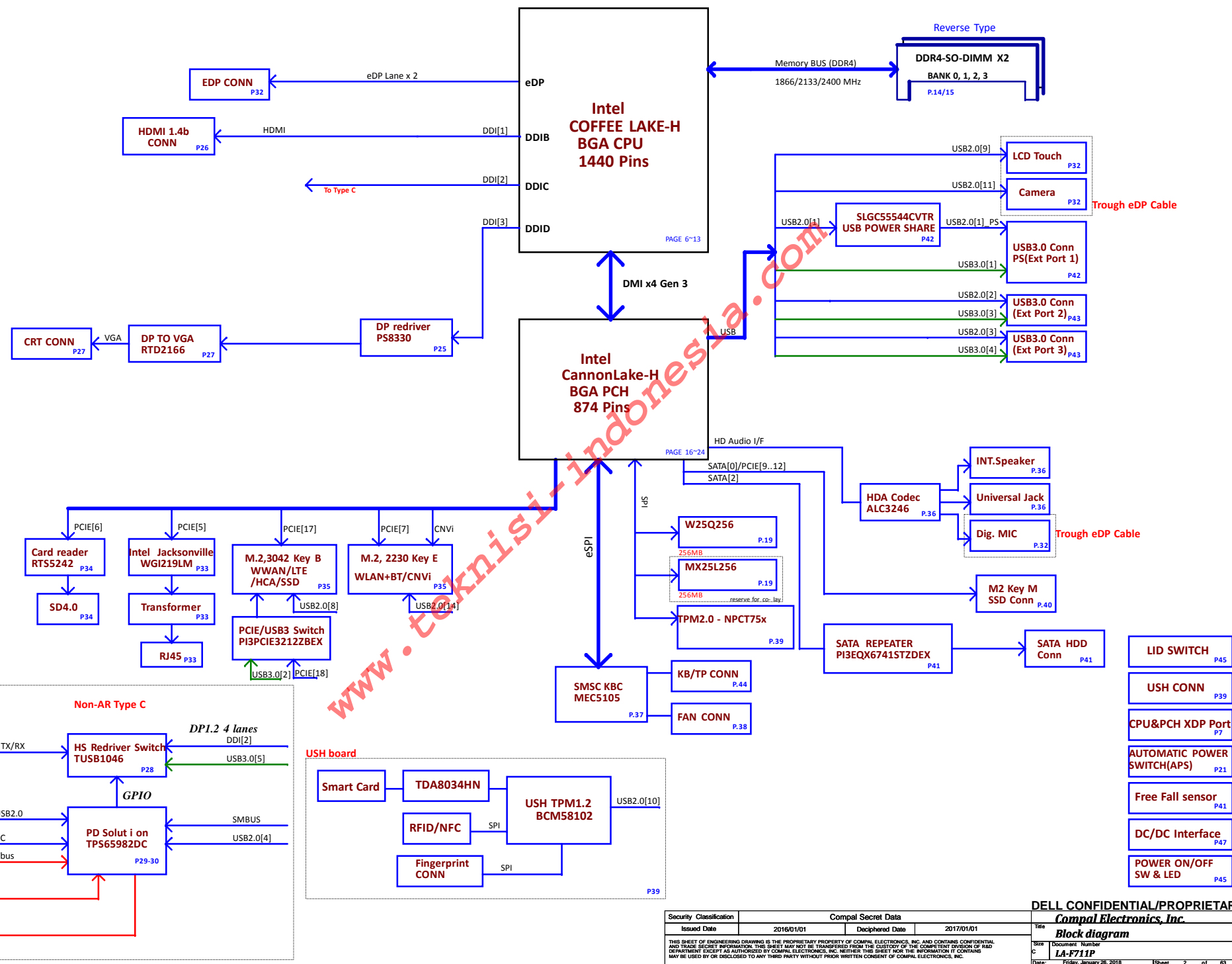
Layout Dell logo



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REV: X02
PWB: GXXF6

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Breckenridge MLK 15 UMA non-TBT Block Diagram



POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_SUS +1.2V_MEM +1.0V_VCCST +2.5V_MEM	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.2V_RUN +VCC_CORE +VCC_GT +1.0VS_VCCIO +VCC_SA +1.8V_RUN
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	IT-158	0.50
			Add Plating		0.95
1	Top		Copper foil	0.5oz	0.65
		3.7	Prepreg	1080	2.60
2	GND1		Copper foil	1oz	1.35
		3.7	Core	4mil	4.00
3	Sig1		Copper foil	1oz	1.35
		3.6	Prepreg	216HRCx2	5.90
4	GND1/PWR		Copper foil	1oz	1.35
		3.7	Core	4mil	4.00
5	Sig2		Copper foil	1oz	1.35
		3.6	Prepreg	216HRCx2	5.20
6	Sig3		Copper foil	1oz	1.35
		3.6	Core	4mil	4.00
7	GND2		Copper foil	1oz	1.35
		3.7	Prepreg	1080	2.60
8	Bottom		Copper foil	0.5oz	0.65
			Add Plating		0.95
			SolderMask		0.50
Overall Thickness (1.2mm ± 10%)				47.2	46.60000 1.18364

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) Type and Lane	USB3.1 #1	USB3.1 #3	USB3.1 #4	USB3.1 #5	USB3.1 #6	USB3.1 #7	USB3.1 #8	USB3.1 #9	USB3.1 #10	PCIe #4	PCIe #5	PCIe #7	PCIe #8	PCIe #9	PCIe #10	PCIe #11	SATA 0a	SATA 1a	SATA 1b	SATA 2	SATA 3	SATA 4	SATA 5	PCIe #18	PCIe #19	PCIe #20	PCIe #21	PCIe #22	PCIe #23	PCIe #24
Intel® RST Support							No Support	No Support						Yes	No Support	Yes							Yes		Yes					

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB1-->Right
USB3.0-2	SSIC-1			JNGFF2-->M2 3042(LTE)
USB3.0-3	SSIC-2			JUSB2-->LEFT
USB3.0-4				JUSB3-->REAR
USB3.0-5				JUSBC1-->TypeC
USB3.0-6				NA
USB3.0-7		PCIE-1		NA
USB3.0-8		PCIE-2		
USB3.0-9		PCIE-3		
USB3.0-10		PCIE-4		
		PCIE-5		LOM
		PCIE-6		Card Reader
		PCIE-7		JNGFF1-->M.2 2230(WLAN)
		PCIE-8		NA
		PCIE-9		M.2 Socket 3 (Key M) M.2 2280 SSD (PCIex4 or SATA)
		PCIE-10		
		PCIE-11	SATA-0A	
		PCIE-12	SATA-1A	
		PCIE-13	SATA-0B	NA
		PCIE-14	SATA-1B	NA
		PCIE-15	SATA-2	JSATA1-->HDD SATA
		PCIE-16	SATA-3	NA
		PCIE-17	SATA-4	M.2 3042 (HCA or QCA LTE) SSD Cache
		PCIE-18	SATA-5	M.2 3042 (HCA or QCA LTE) SSD Cache
		PCIE-19		NA
		PCIE-20		NA

USB PORT#	DESTINATION
1	JUSB1-->Right
2	JUSB2 ->Lef t
3	JUSB3-->Rear
4	Type C
5	NA
6	test point
7	NA
8	JNGFF2-->M2 3042(WWAN)
9	JEDP1-->Touch Screen
10	JUSH1-->USH
11	JEDP1-->Camera
12	NA
13	NA
14	JNGFF1--> M.2 2230(CNVi_BT)

USH	H	BIO
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VIDEO	DESTINATION
eDP	LCD
DDI-B	JHDMI1
DDI-C	Type-C
DDI-D	MB VGA

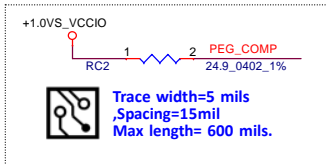
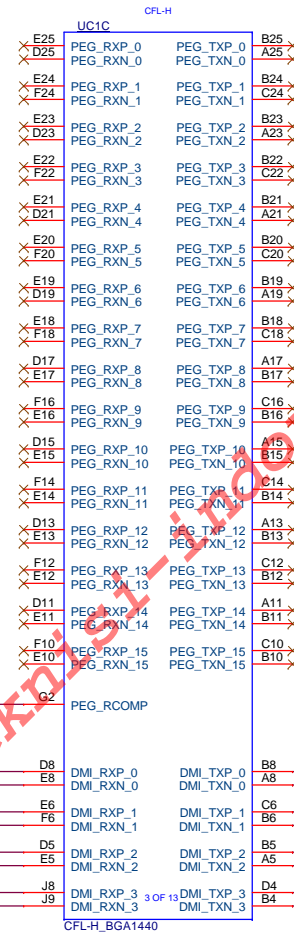
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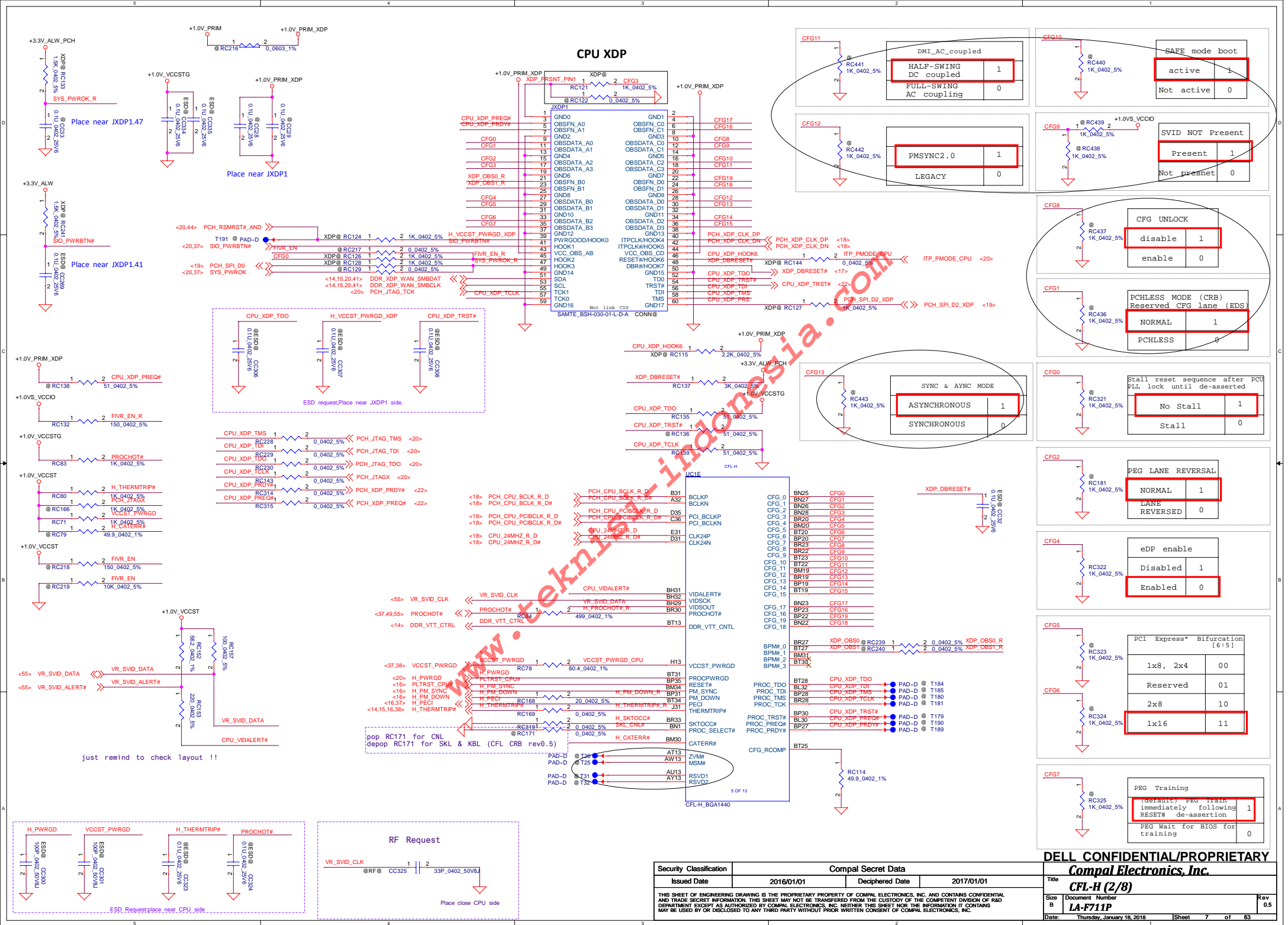
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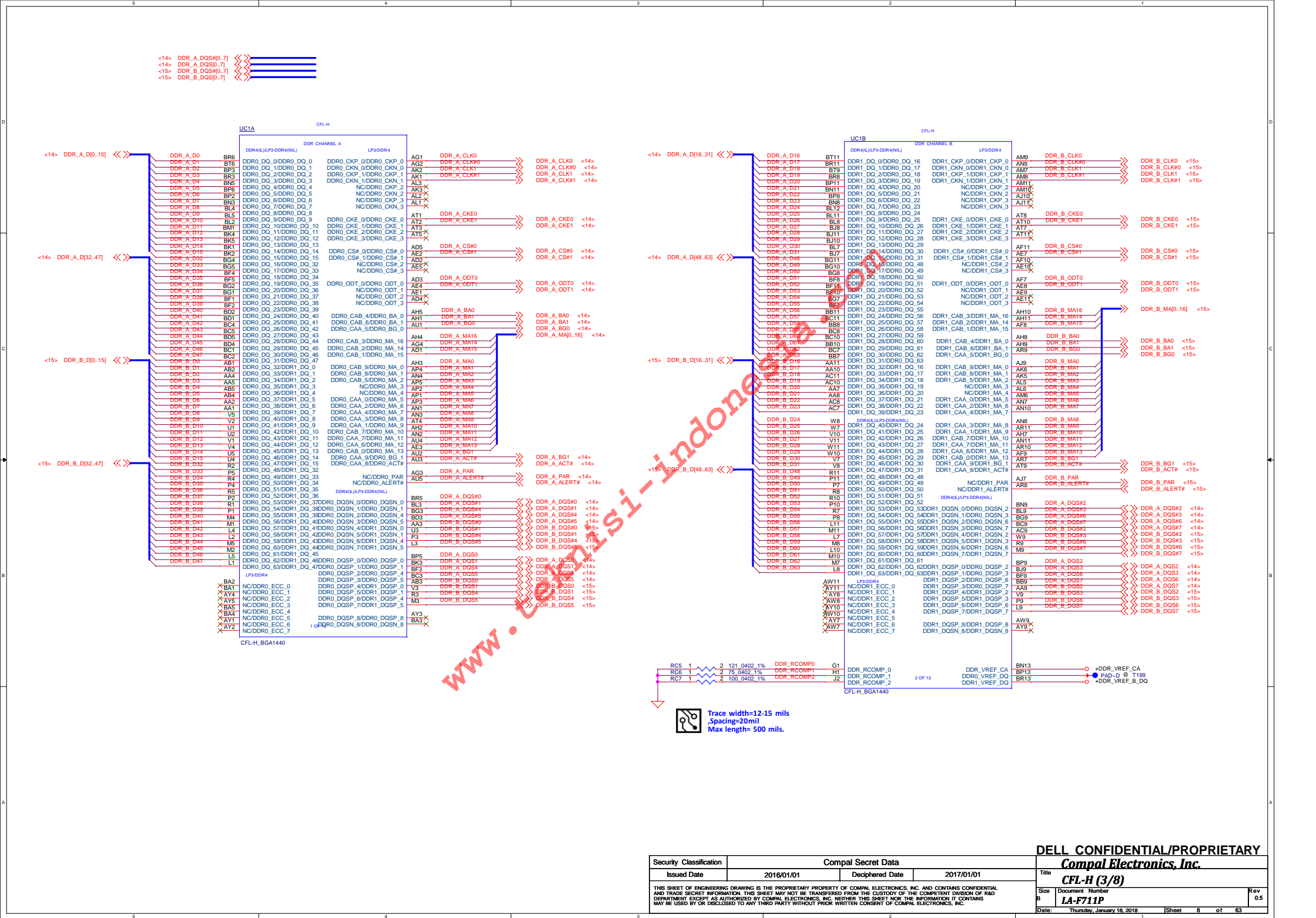
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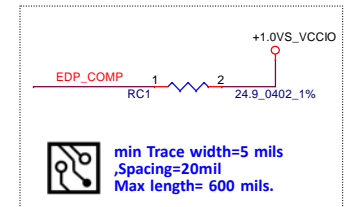
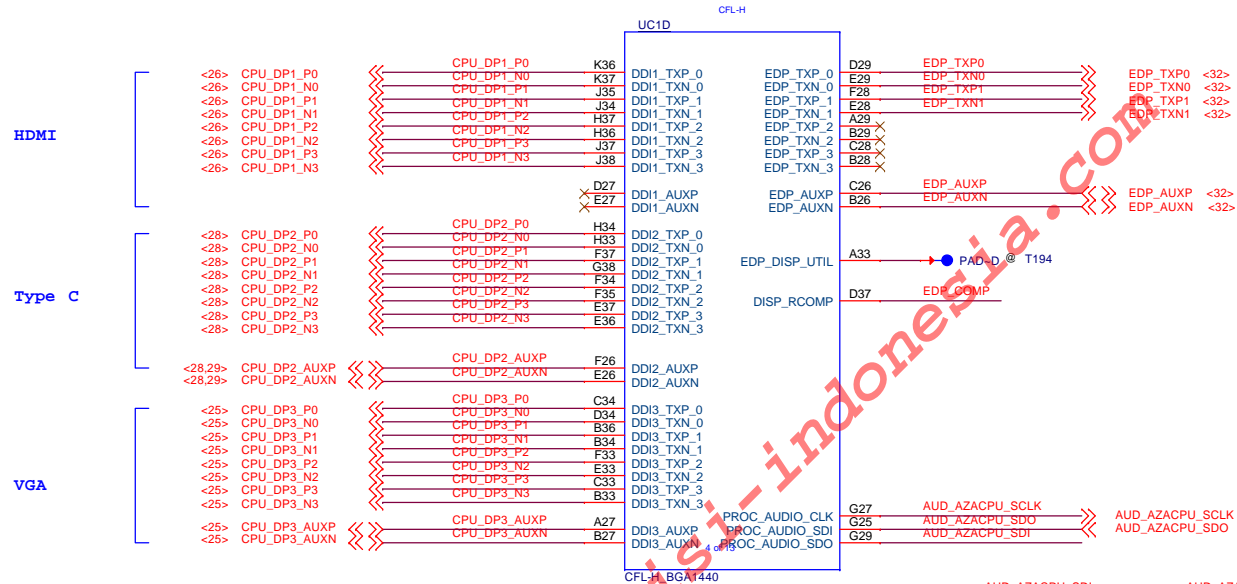
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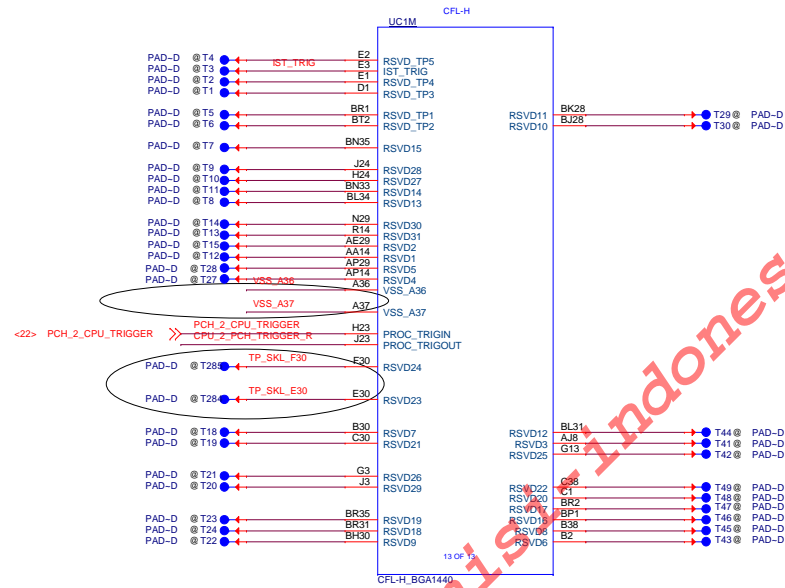




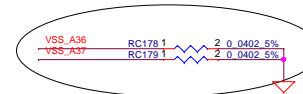


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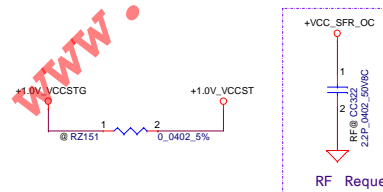
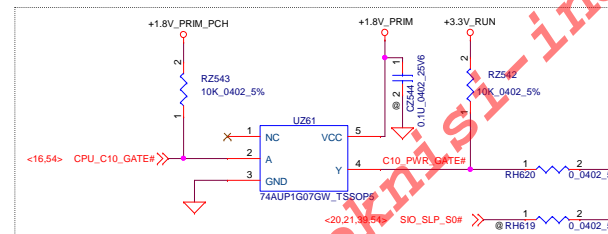
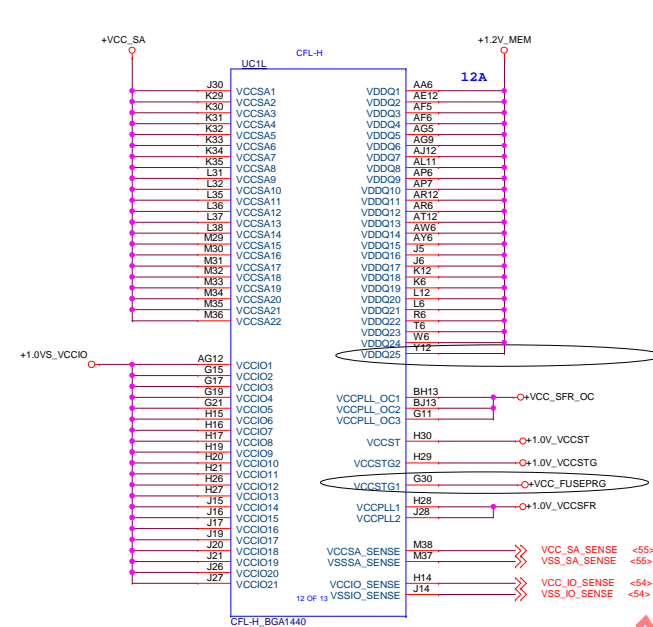
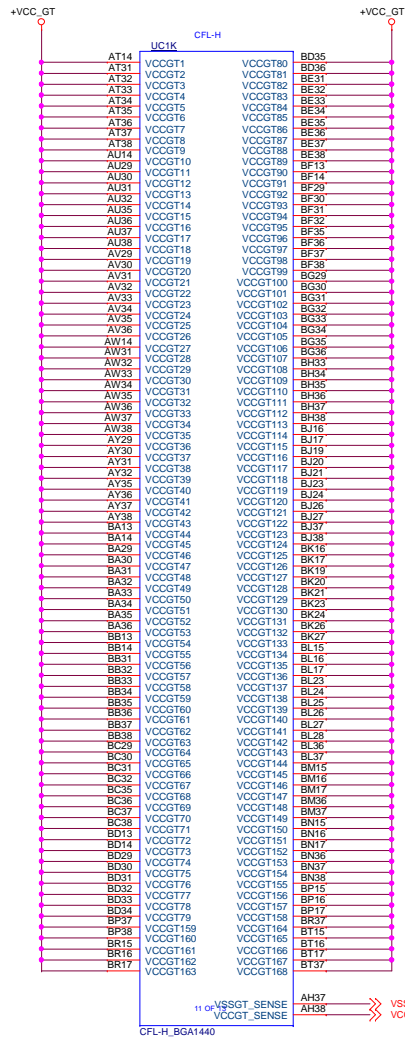
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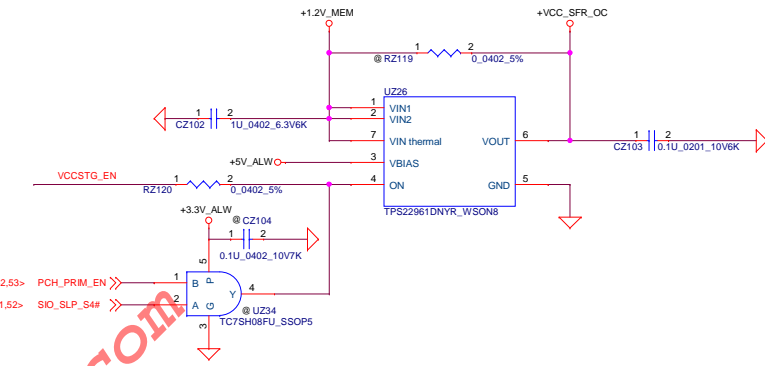
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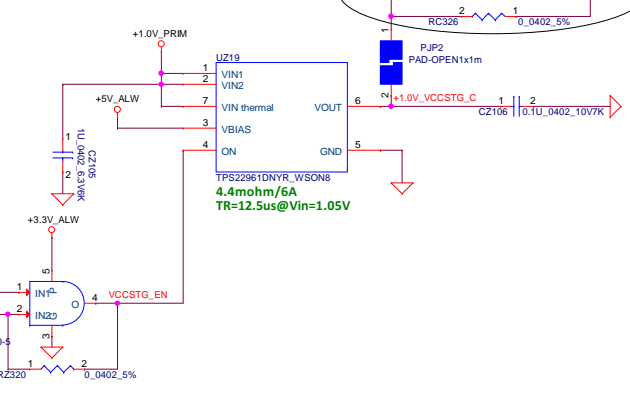
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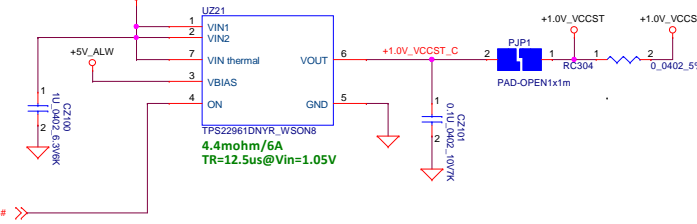
+VCCPLL_OC source



+1.0V_VCCSTG source



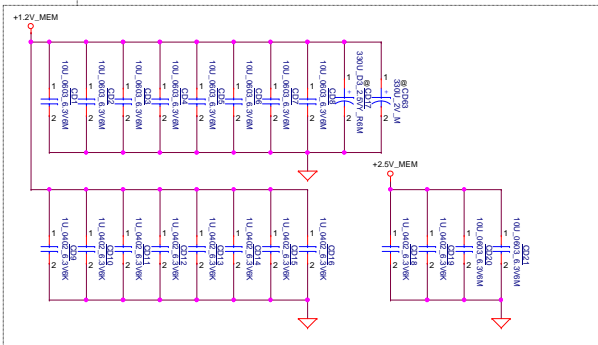
+1.0V_VCCST source



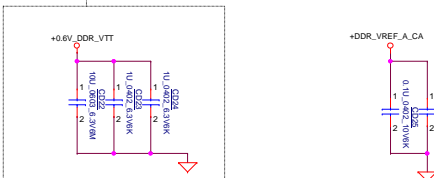
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 DDR_A_DQS#(0..7)
 DDR_A_DQS(0..7)
 DDR_A_DQ(15)
 DDR_A_DQ(16..31)
 DDR_A_DQ(32..47)
 DDR_A_DQ(48..63)
 DDR_A_MA(0..16)

Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.258

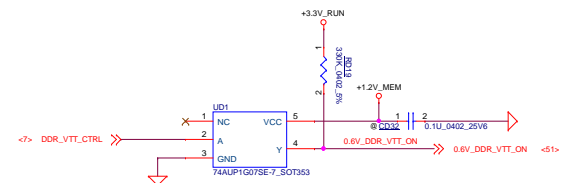
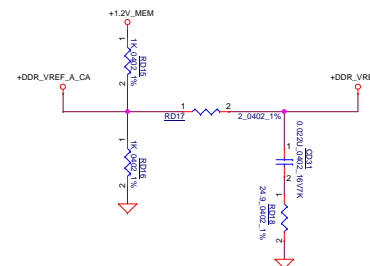
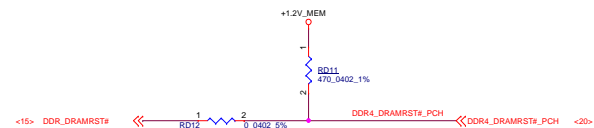
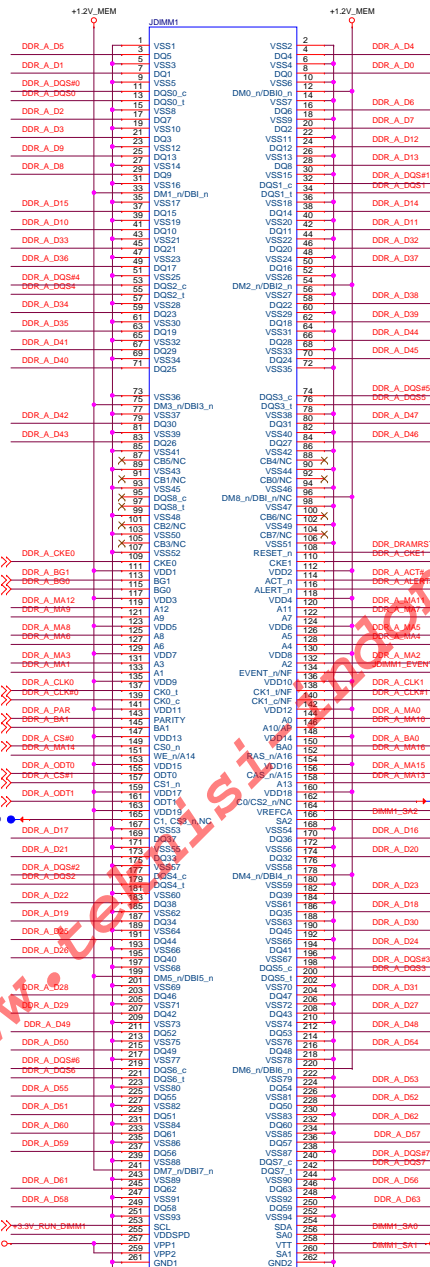


DIMM Select

	SA0	SA1	SA2
* DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0

Byte[0]	DQ[7:0]	DQS/DQS#[0]
Byte[1]	DQ[15:8]	DQS/DQS#[1]
Byte[2]	DQ[23:16]	DQS/DQS#[2]
* Byte[3]	DQ[31:24]	DQS/DQS#[3]
Byte[4]	DQ[39:32]	DQS/DQS#[4]
* Byte[5]	DQ[47:40]	DQS/DQS#[5]
Byte[6]	DQ[55:48]	DQS/DQS#[6]
Byte[7]	DQ[63:56]	DQS/DQS#[7]

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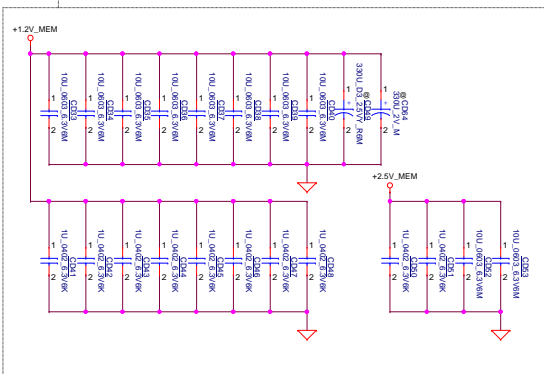
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DDR4-SODIMM SLOT1

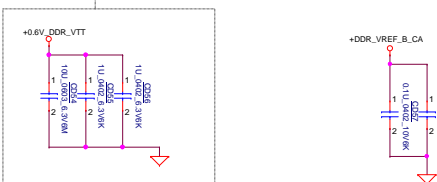
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 DDR_B_DQS#0..7
 DDR_B_DQS#0..7
 DDR_B_DQ0..15
 DDR_B_DQ16..31
 DDR_B_DQ32..47
 DDR_B_DQ48..63
 DDR_B_MA0..16

Layout Note:
Place near J1MM2

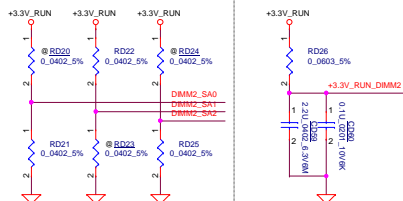


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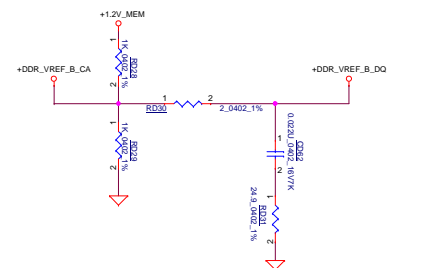
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DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0

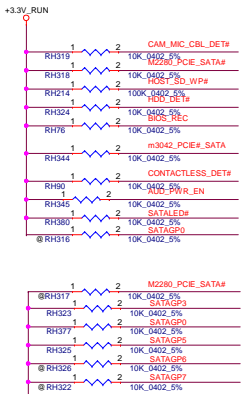


Byte[0]	DQ[7:0]	DQS/DQS#[0]
Byte[1]	DQ[15:8]	DQS/DQS#[1]
Byte[2]	DQ[23:16]	DQS/DQS#[2]
Byte[3]	DQ[31:24]	DQS/DQS#[3]
Byte[4]	DQ[39:32]	DQS/DQS#[4]
Byte[5]	DQ[47:40]	DQS/DQS#[5]
Byte[6]	DQ[55:48]	DQS/DQS#[6]
Byte[7]	DQ[63:56]	DQS/DQS#[7]

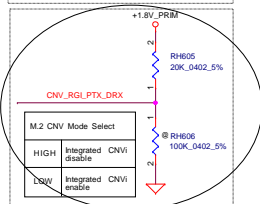


J1MM2_EVENTS 1 2 1K,0402,5% H_THERMTRIP# <7,14,16,38>

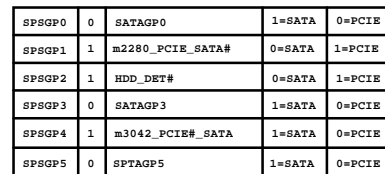


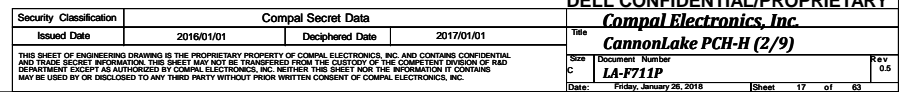
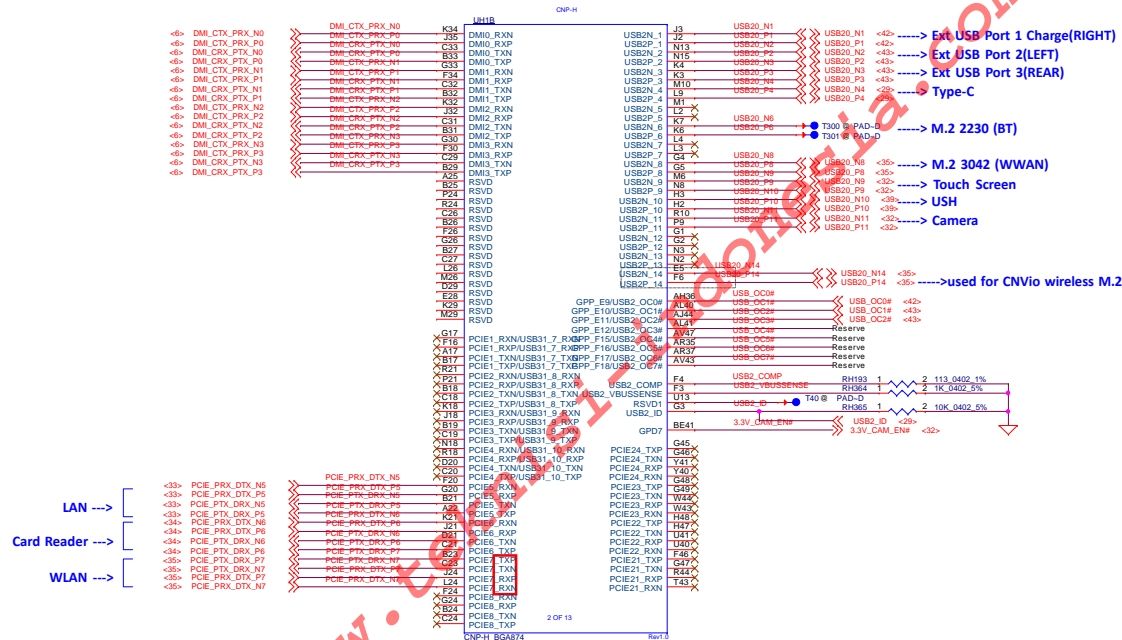


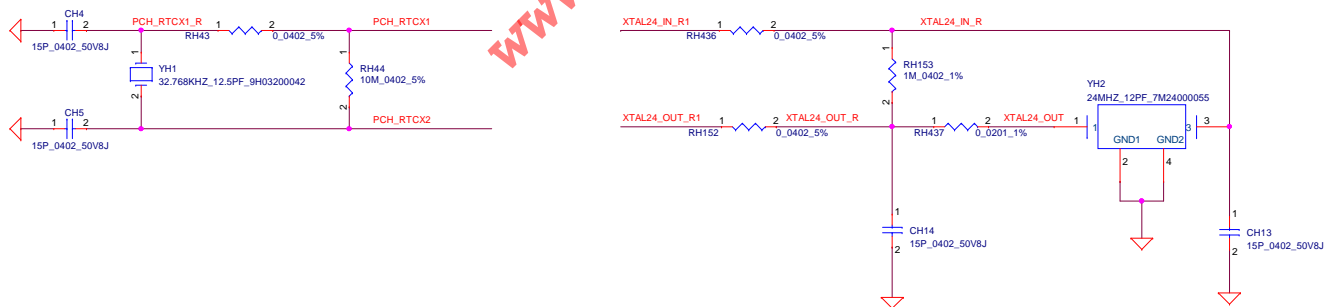
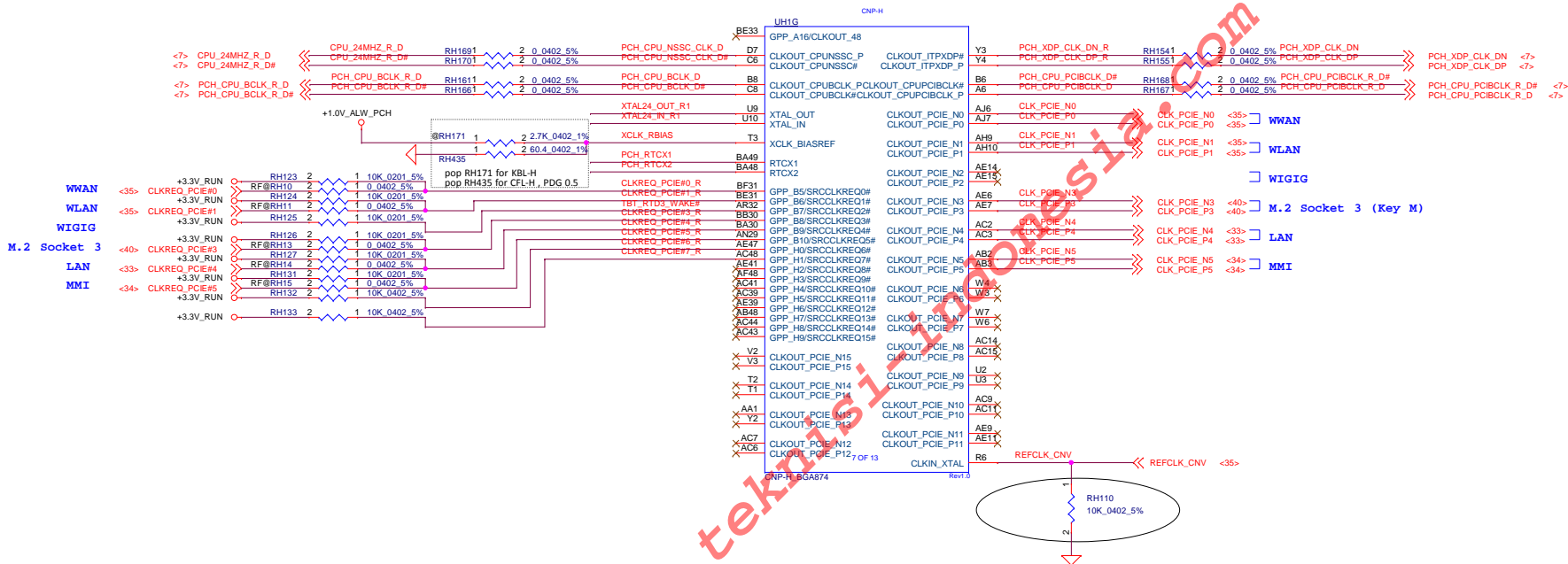
M.2 Socket 3 (Key M)



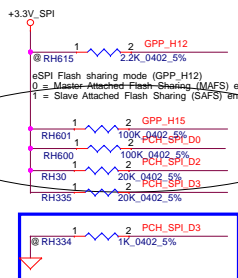
M.2 3042 HCA or QCA LTE SSD Cache







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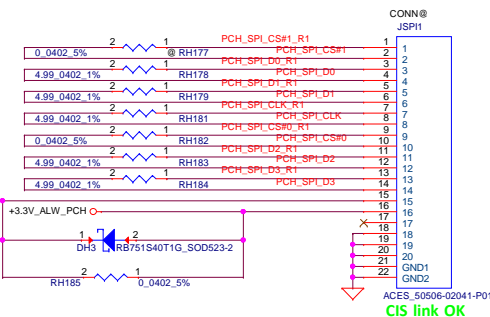
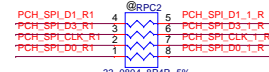
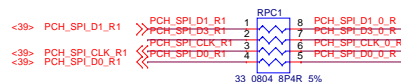
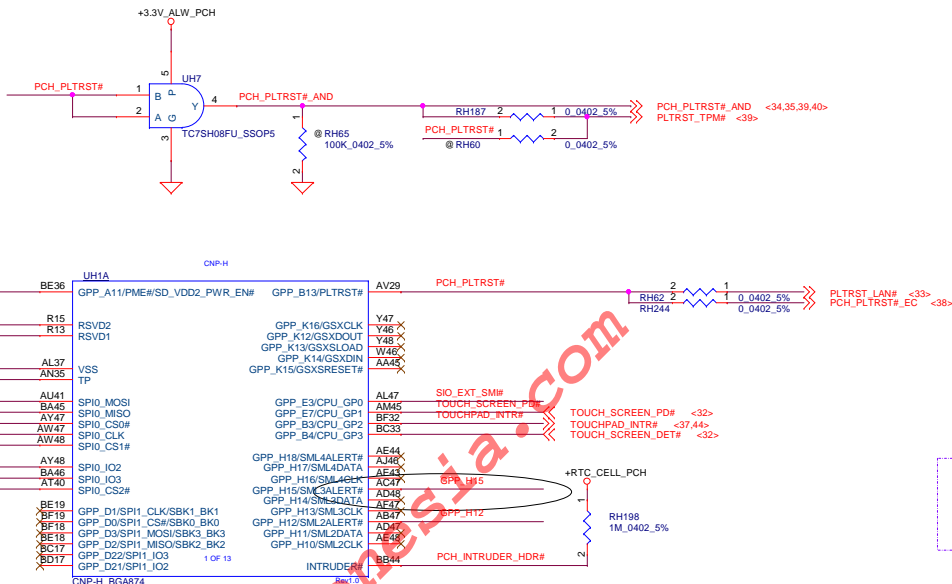
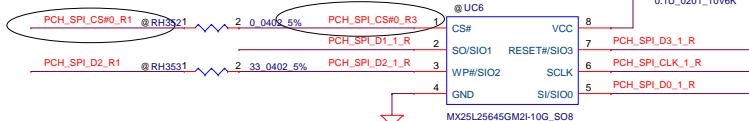
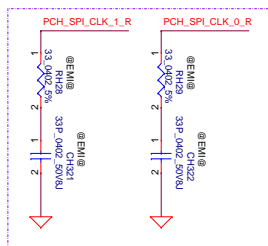
CFL-H PDG rev0.7
pop 20K for SPI0_IO2/3

CNL- PCH EDS rev0.5
Reserved External pull-up is required. Recommend 100K if pulled
up to 3.3V

Option 1: Implement a 1kOhm pull-down resistor on the signal and de-populate the required 1kOhm pull-up resistor. In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.

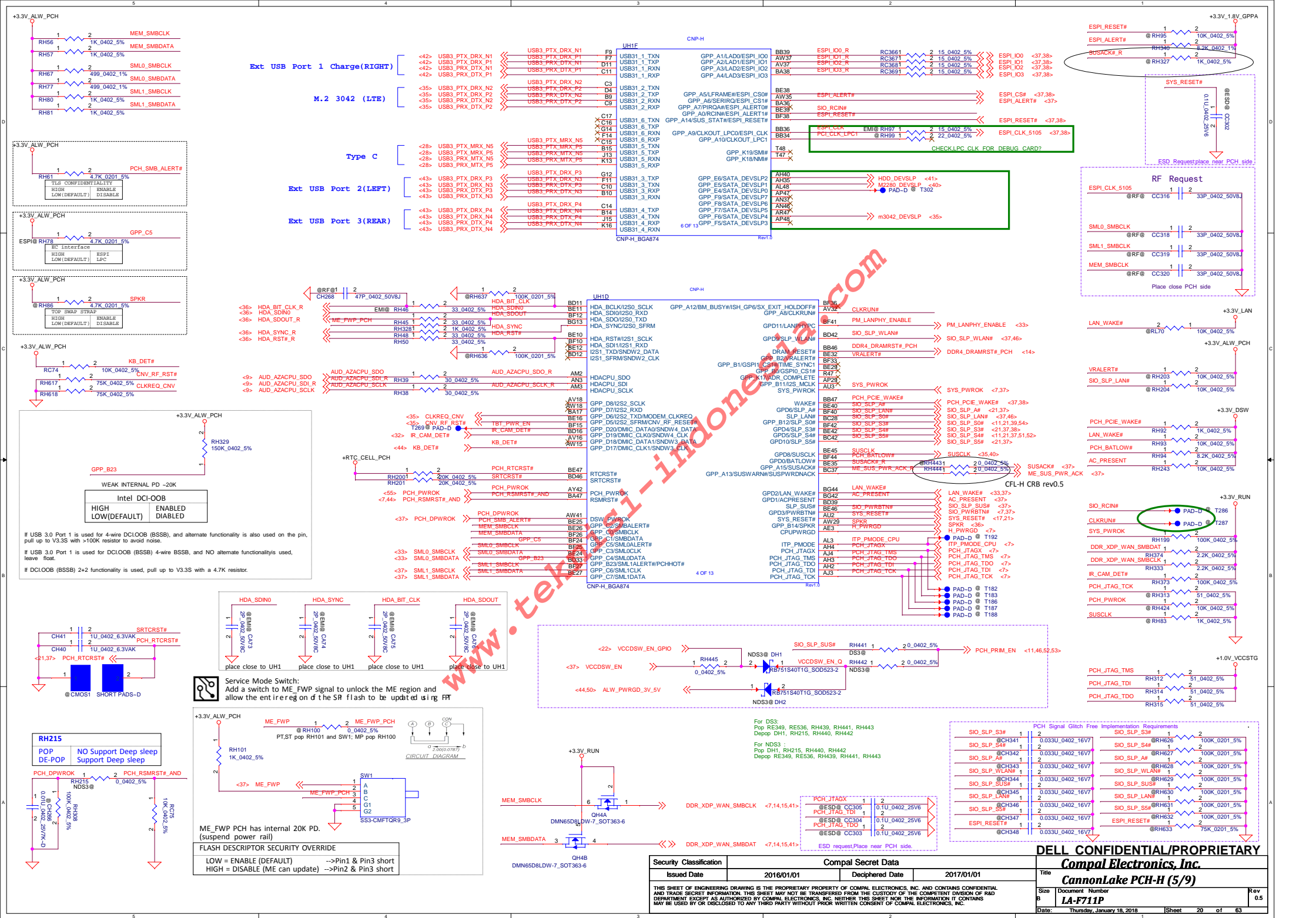
Note that the pull down resistor on SPI0_IO3 is only needed for SKL U/Y plat f or rs with ES and SKL S/H plat f or rs with pre-ES1/ES1 sa mp les.

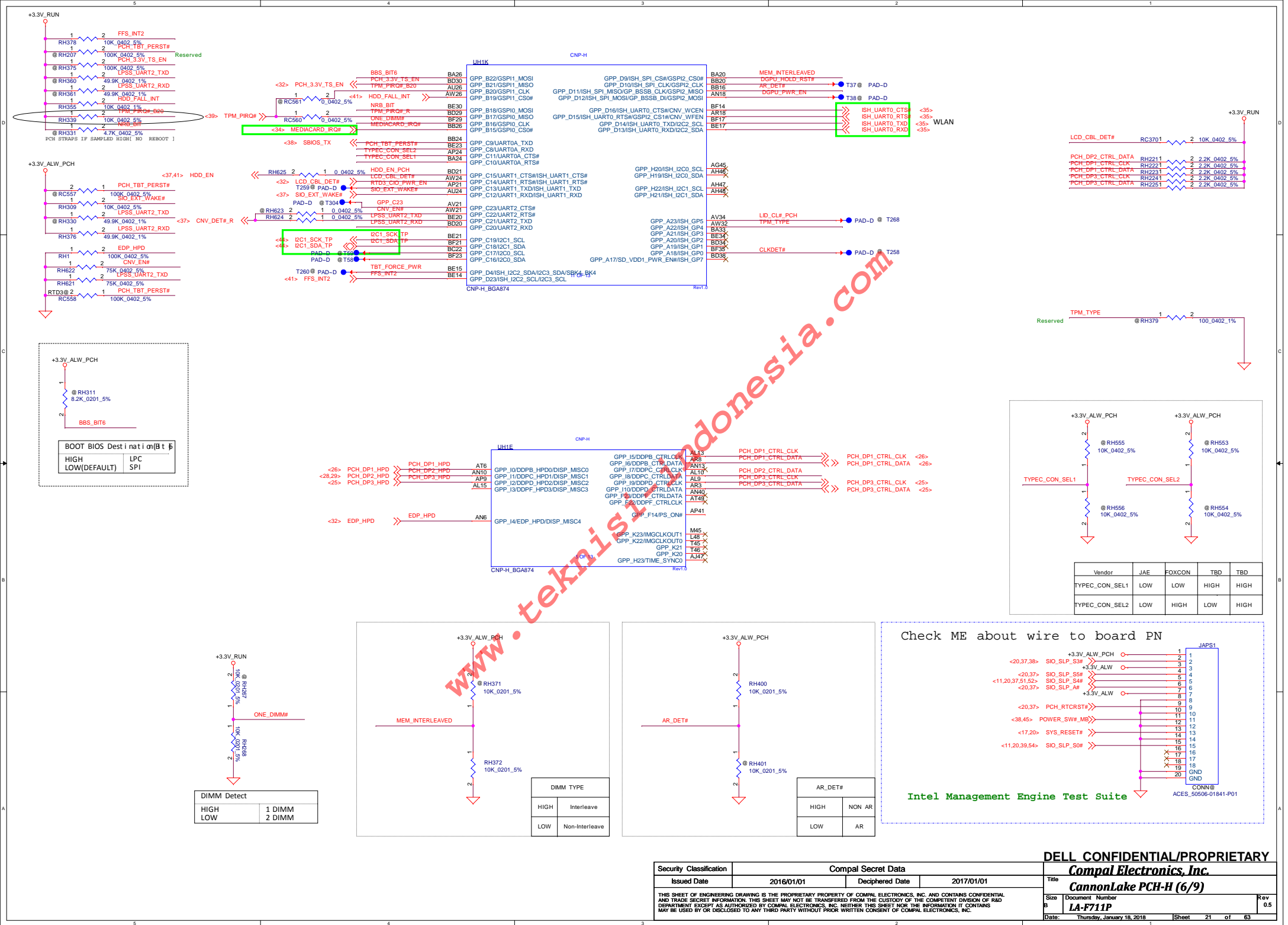
	ESPI	LPC
RH351	33 ohm	15 ohm
RPC1	33 ohm	15 ohm
RH178, RH179, RH181 RH182, RH183, RH184	0 ohm	25 ohm

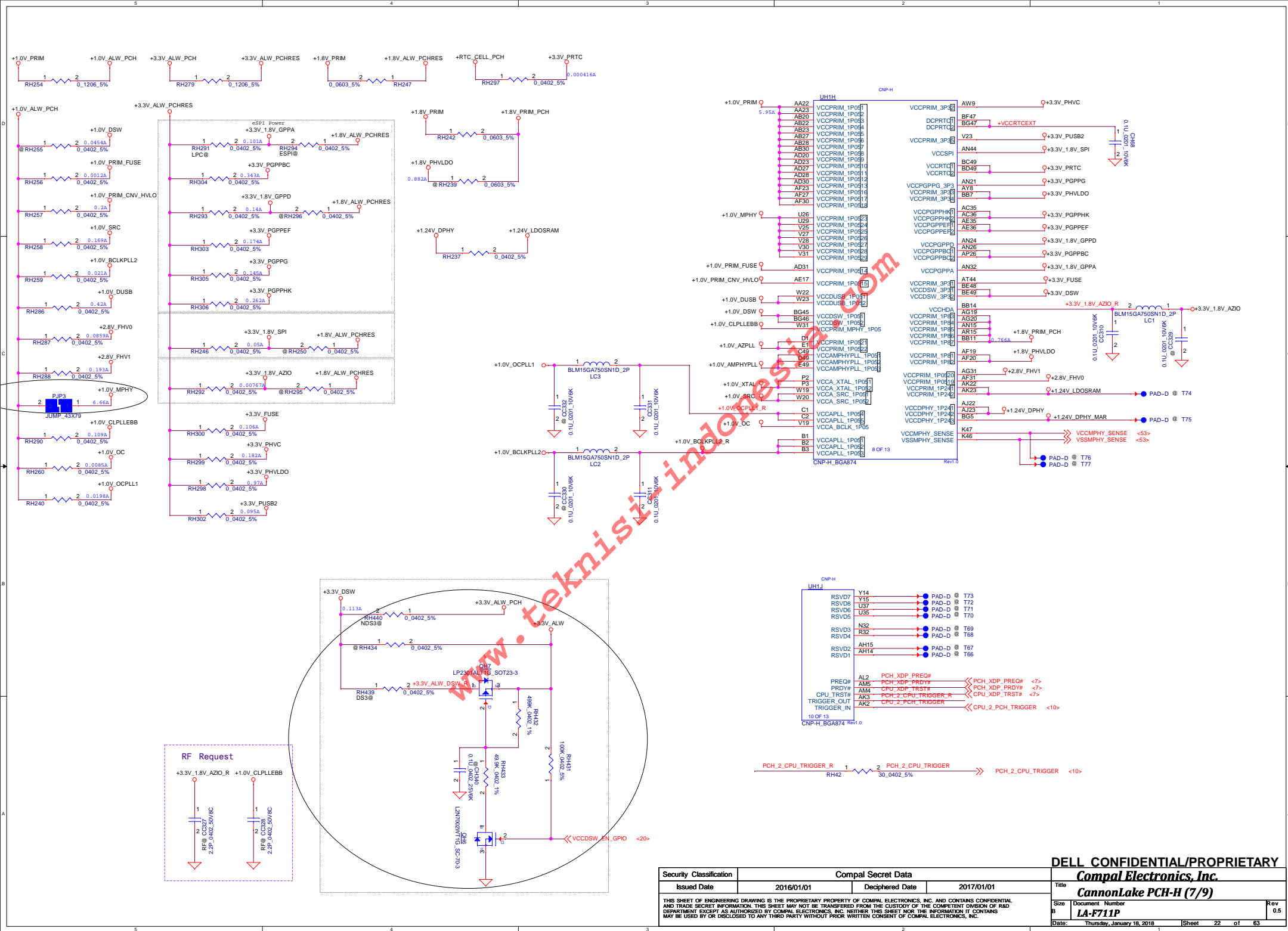


ACES_50506-02041-P01
CIS link OK

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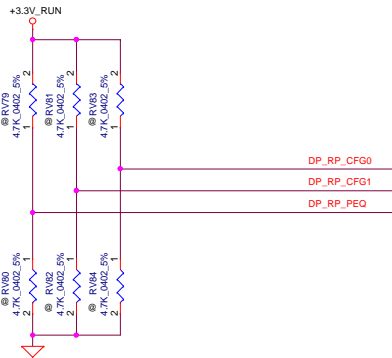
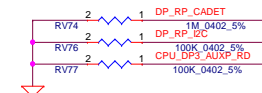
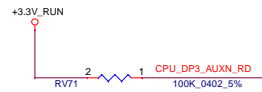


CNP-H			
UH1L		UH1L	
A2	VSS	AL12	VSS
A28	VSS	AL17	VSS
A3	VSS	AL21	VSS
A33	VSS	AL24	VSS
A37	VSS	AL26	VSS
A4	VSS	AL28	VSS
A45	VSS	AL33	VSS
A46	VSS	AL38	VSS
A47	VSS	AM1	VSS
A48	VSS	AM18	VSS
A5	VSS	AM32	VSS
A8	VSS	AM40	VSS
AA19	VSS	AN12	VSS
AA20	VSS	AN16	VSS
AA25	VSS	AN34	VSS
AA27	VSS	AN38	VSS
AA28	VSS	AP4	VSS
AA30	VSS	AP46	VSS
AA31	VSS	AR12	VSS
AA49	VSS	AR16	VSS
AA5	VSS	AR34	VSS
AB19	VSS	AR38	VSS
AB25	VSS	AT1	VSS
AB31	VSS	AT16	VSS
AC12	VSS	AT18	VSS
AC17	VSS	AT21	VSS
AC33	VSS	AT24	VSS
AC38	VSS	AT26	VSS
AC4	VSS	AT29	VSS
AC46	VSS	AT32	VSS
AD1	VSS	AT34	VSS
AD19	VSS	AT45	VSS
AD2	VSS	AV11	VSS
AD22	VSS	AV39	VSS
AD25	VSS	AW10	VSS
AD49	VSS	AW4	VSS
AE12	VSS	AW40	VSS
AE33	VSS	AW45	VSS
AE38	VSS	B47	VSS
AE4	VSS	B48	VSS
AE46	VSS	B49	VSS
AF22	VSS	BA12	VSS
AF25	VSS	BA14	VSS
AF28	VSS	BA44	VSS
AG1	VSS	BA5	VSS
AG22	VSS	BA6	VSS
AG23	VSS	BB41	VSS
AG25	VSS	BB43	VSS
AG27	VSS	BB9	VSS
AG28	VSS	BC10	VSS
AG30	VSS	BC13	VSS
AG49	VSS	BC15	VSS
AH12	VSS	BC19	VSS
AH17	VSS	BC24	VSS
AH33	VSS	BC26	VSS
AH38	VSS	BC31	VSS
AJ19	VSS	BC35	VSS
AJ20	VSS	BC40	VSS
AJ25	VSS	BC45	VSS
AJ27	VSS	BC6	VSS
AJ28	VSS	BD43	VSS
AJ30	VSS	BE44	VSS
AJ31	VSS	BF1	VSS
AK19	VSS	BF2	VSS
AK20	VSS	BF3	VSS
AK25	VSS	BF48	VSS
AK27	VSS	BF49	VSS
AK28	VSS	BG17	VSS
AK30	VSS	BG2	VSS
AK31	VSS	BG22	VSS
AK4	VSS	BG25	VSS
AK46	VSS	BG28	VSS

9 OF 13
CNP-H_BGA874 Rev1.3

CNP-H			
UH1L		UH1L	
BG3	VSS	M24	VSS
BG33	VSS	M32	VSS
BG37	VSS	M34	VSS
BG4	VSS	M49	VSS
BG46	VSS	M5	VSS
C12	VSS	N12	VSS
C25	VSS	N16	VSS
C30	VSS	N34	VSS
C4	VSS	N35	VSS
C48	VSS	N37	VSS
C5	VSS	N38	VSS
D12	VSS	P26	VSS
D16	VSS	P29	VSS
D17	VSS	P4	VSS
D30	VSS	P46	VSS
D33	VSS	R12	VSS
D6	VSS	R16	VSS
E10	VSS	R26	VSS
E13	VSS	R29	VSS
E15	VSS	R3	VSS
E17	VSS	R34	VSS
E19	VSS	R38	VSS
E2	VSS	R4	VSS
E24	VSS	T17	VSS
E26	VSS	T18	VSS
E31	VSS	T32	VSS
E33	VSS	T4	VSS
E35	VSS	T49	VSS
E38	VSS	T5	VSS
E40	VSS	T7	VSS
E42	VSS	U12	VSS
E8	VSS	U15	VSS
F41	VSS	U17	VSS
F43	VSS	U21	VSS
F47	VSS	U24	VSS
G44	VSS	U33	VSS
G6	VSS	U38	VSS
H6	VSS	V20	VSS
J10	VSS	V22	VSS
J26	VSS	V4	VSS
J29	VSS	V46	VSS
J4	VSS	W25	VSS
J40	VSS	W27	VSS
J46	VSS	W28	VSS
J47	VSS	W30	VSS
J48	VSS	Y10	VSS
J9	VSS	Y12	VSS
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M16	VSS	Y38	VSS
M18	VSS	Y9	VSS
M21	VSS		

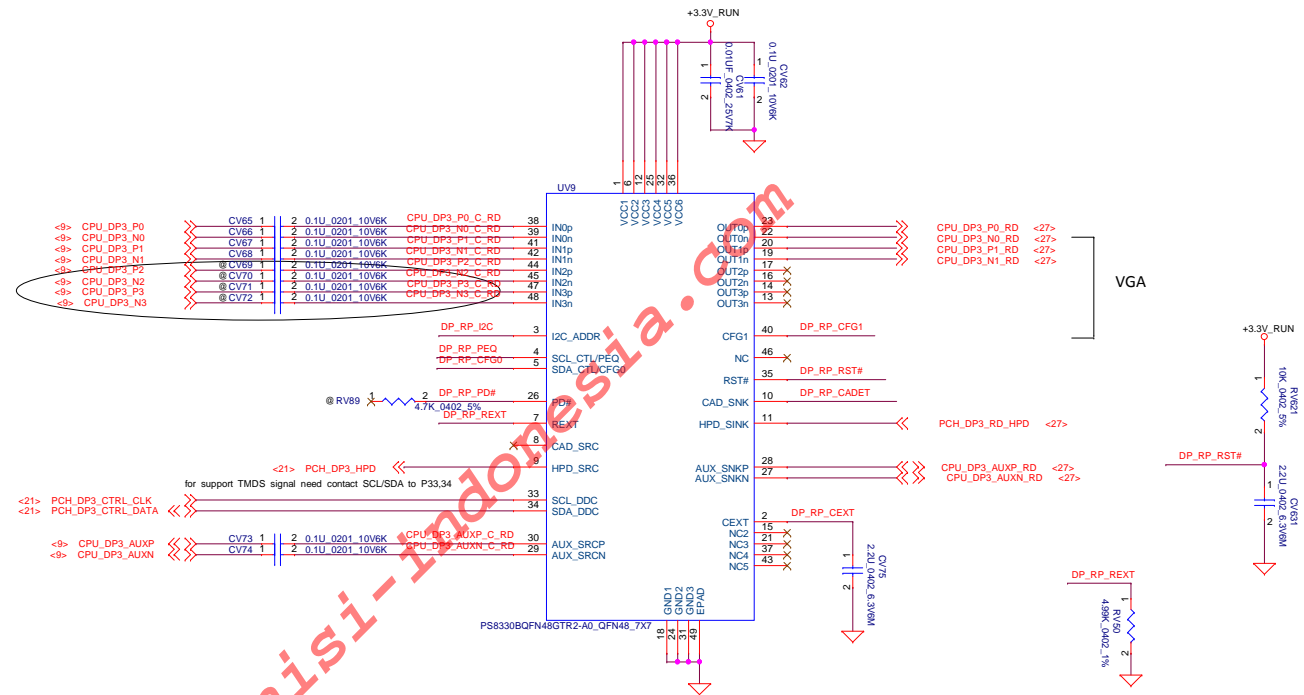
12 OF 13
CNP-H_BGA874 Rev1.3



DP_RP_CFG0 :
Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150k Ω , 3.3V I/O
L: default, automatic EQ enable & AUX interception enable
H: automatic EQ disable & AUX interception enable
M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing

DP_RP_CFG1 :
Configuration pin for auto test and input offset cancellation, 3.3V I/O, internal pull up at ~150k Ω
H: default, auto test disable & input offset cancellation enable
L: auto test enable & input offset cancellation enable
M: auto test disable & input offset cancellation disable

DP_RP_PEQ :
Programmable input equalization levels; Internal pull down at ~150k Ω , 3.3V I/O
L: default, LEQ, compensate channel loss up to 12dB @ HBR2
H: HEQ, compensate channel loss up to 15dB @ HBR2
M: LLEQ, compensate channel loss up to 5dB @ HBR2



VGA

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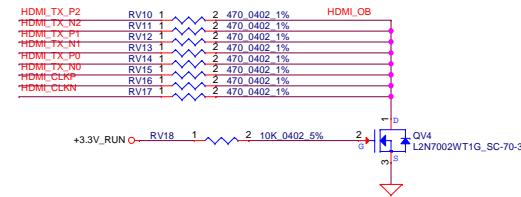
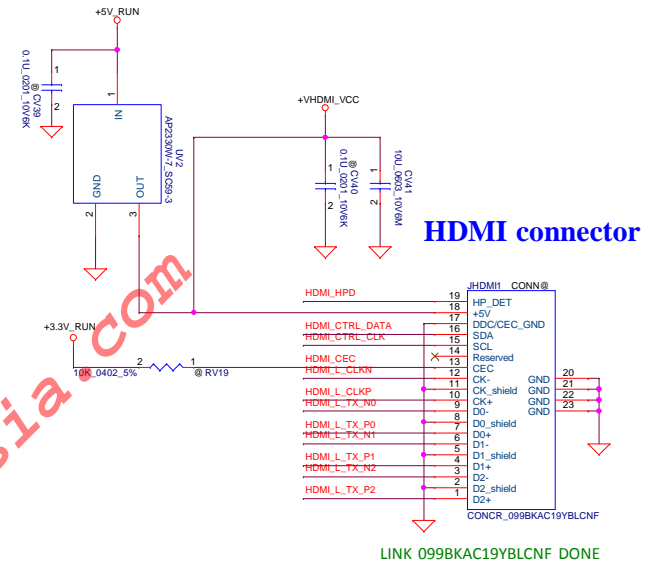
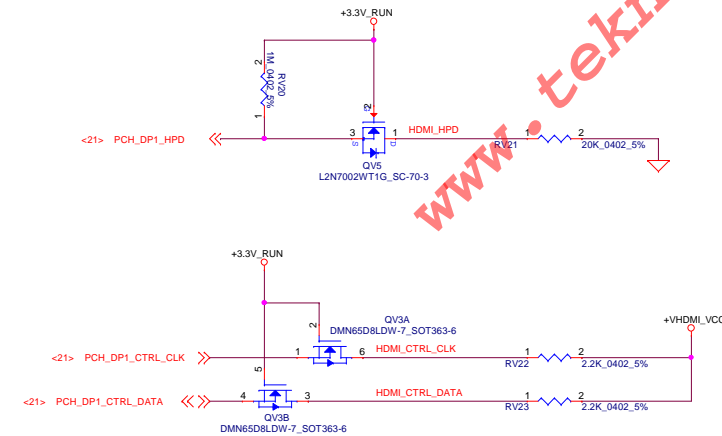
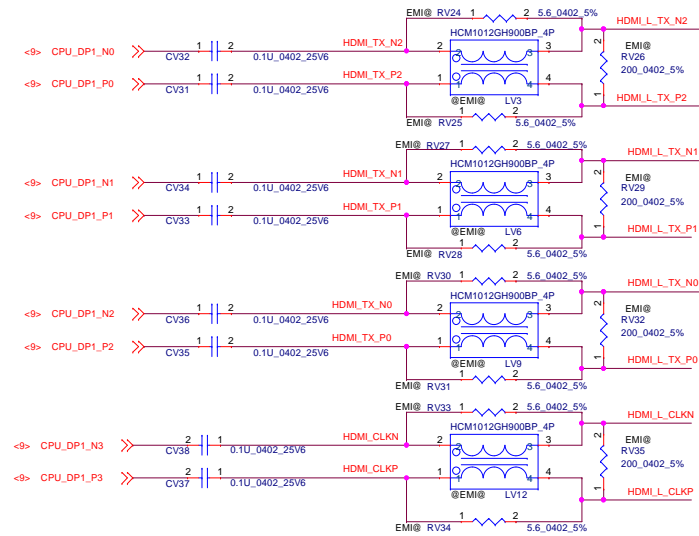
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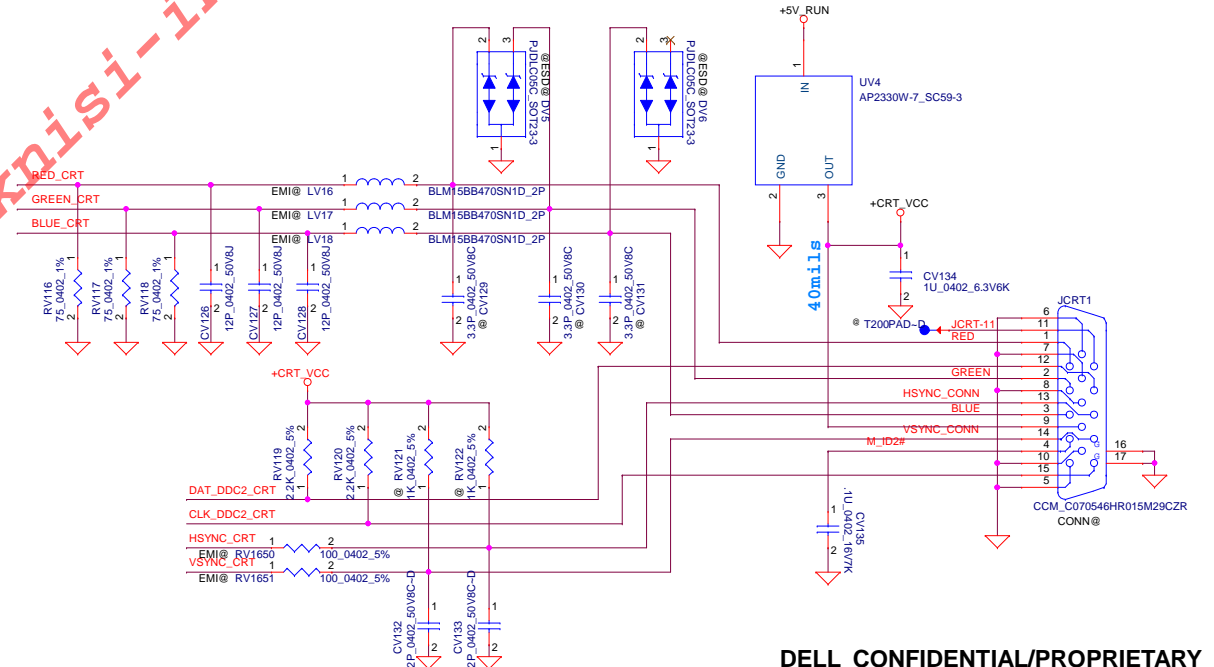
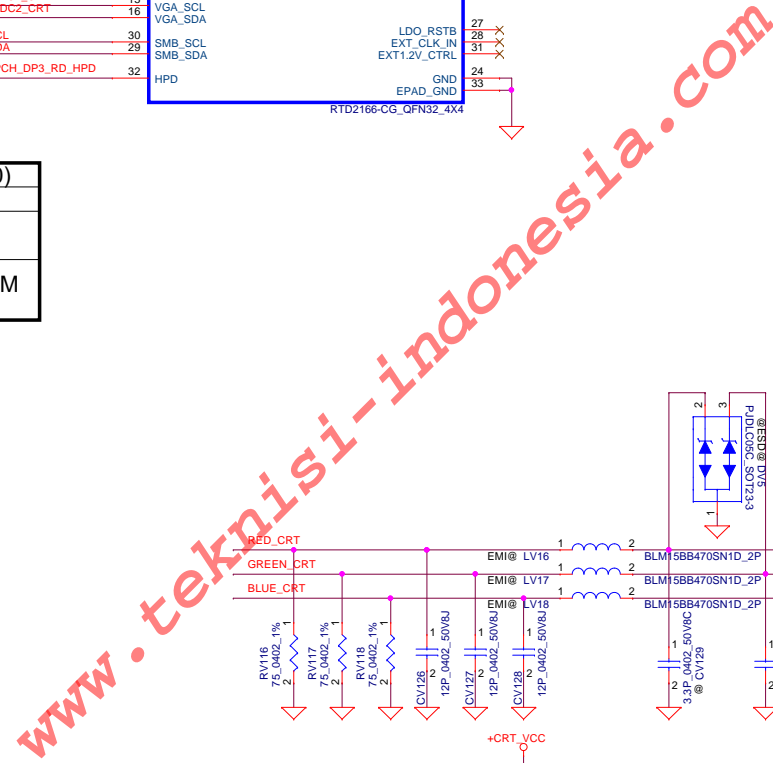
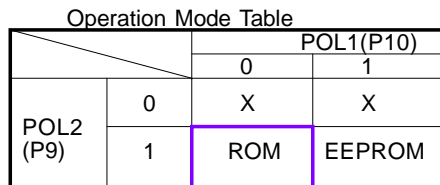
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Size B Document Number LA-F711P Rev 0.5
Date: Thursday, January 18, 2018 Sheet 25 of 63

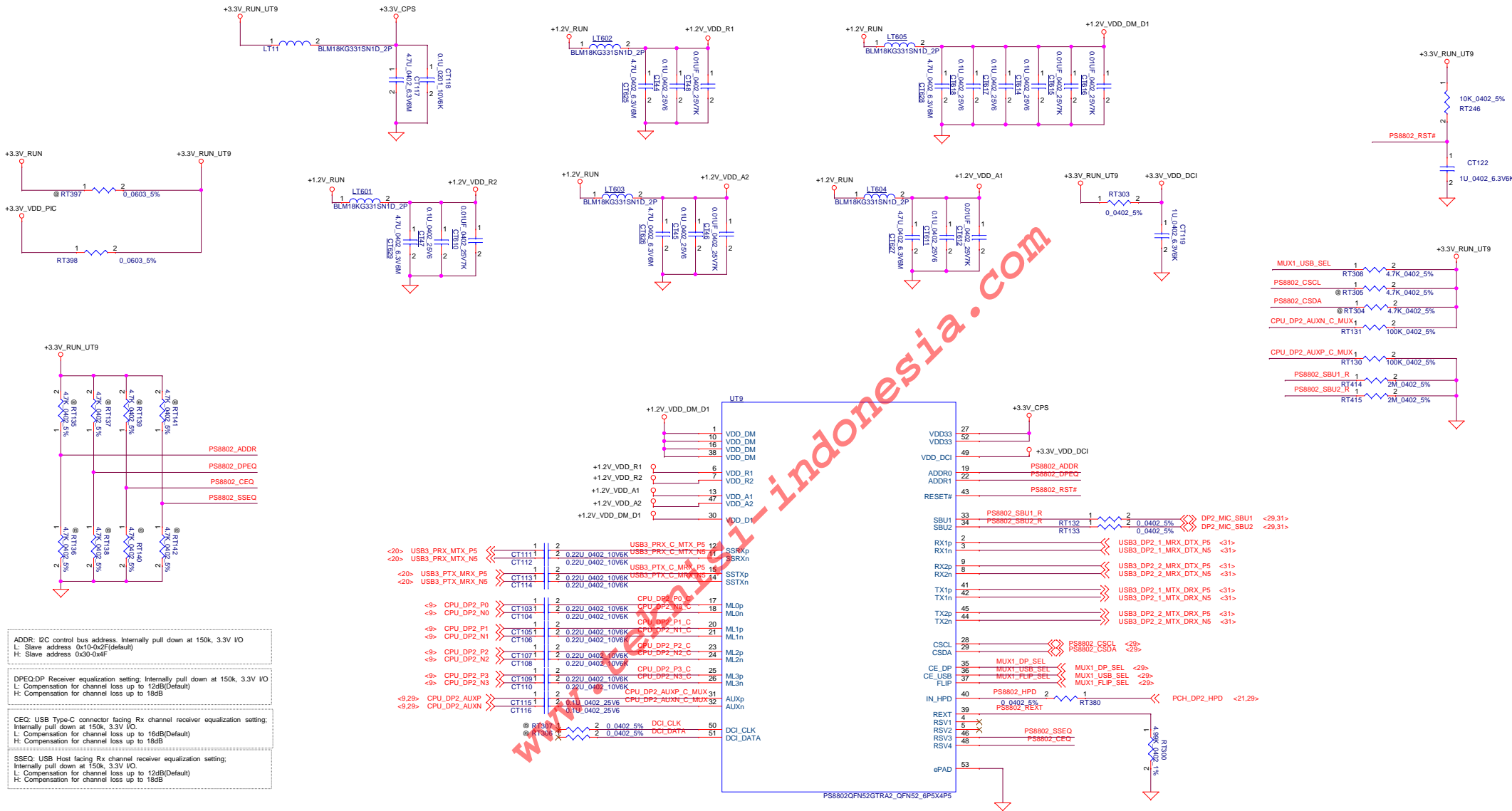
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For Realtek Solution



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				Date	Thursday, January 18, 2018
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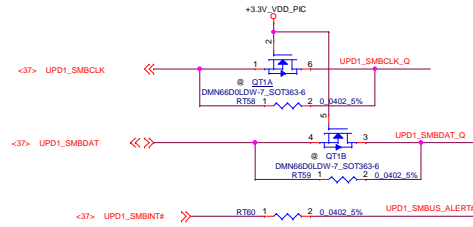
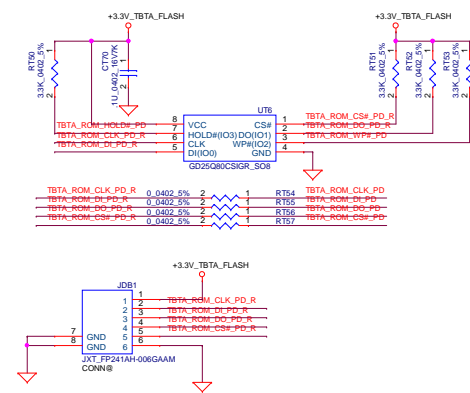
change from SA0000A1M10(A1) to SA0000A1M20(A2)

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Compal Electronics, Inc.						
DP/USB3 Re-timer PS8802						
Size						
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Document Number						
LA-F711P						
Rev						
0.5						
Date: Wednesday, January 31, 2018						
Sheet 28 of 63						

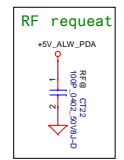
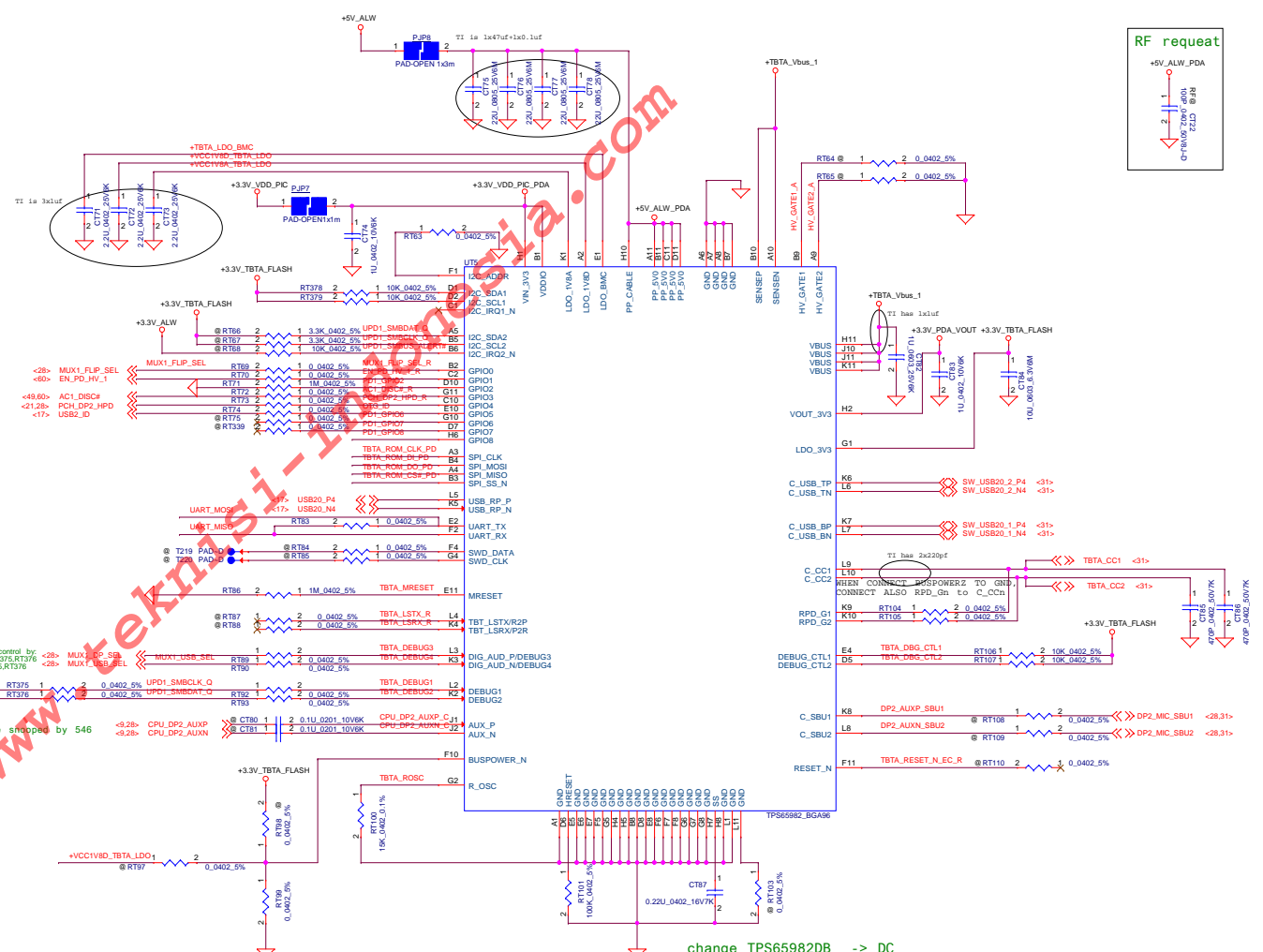
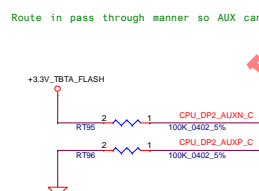
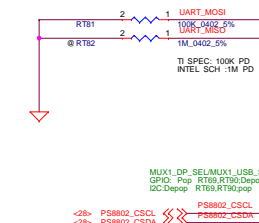
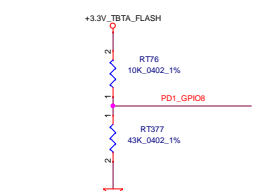
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Compal Electronics, Inc.
DP/USB3 Re-timer PS8802

Document Number
LA-F711P
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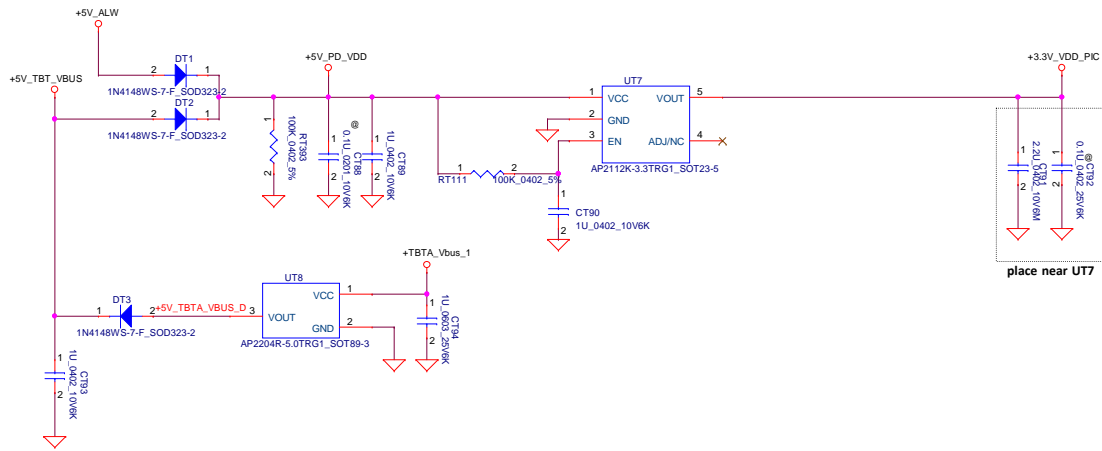
For Non-AR config



DIV = R2/(R1+R2)		Factory Configuration	Description
DIV_min	DIV_max		
0.00	0.08	0	UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9 -3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.10	0.18	1	UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9 -3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.20	0.28	2	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.30	0.38	3	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configuration TI VID supported
0.40	0.48	4	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported Accepts data and power role swaps, but does not initiate.
0.50	0.58	5	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes -Source, C, D, and E pin configurations TI VID supported Accepts power role swaps but will not initiate. Accepts data role swaps to UFP and can initiate.
0.60	0.68	6	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes -Source, C, D, and E pin configurations TI VID supported Accepts power role swaps but will not initiate. Accepts data role swaps to UFP and can initiate.
0.70	1.00	7	Infinite host retry from Flash to Host IF cycles.



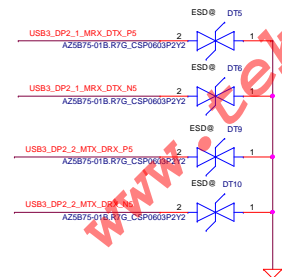
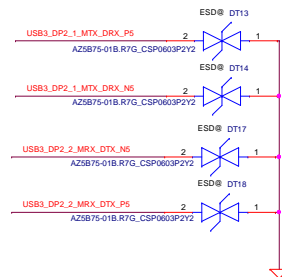
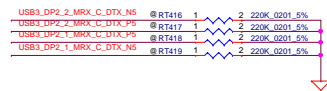
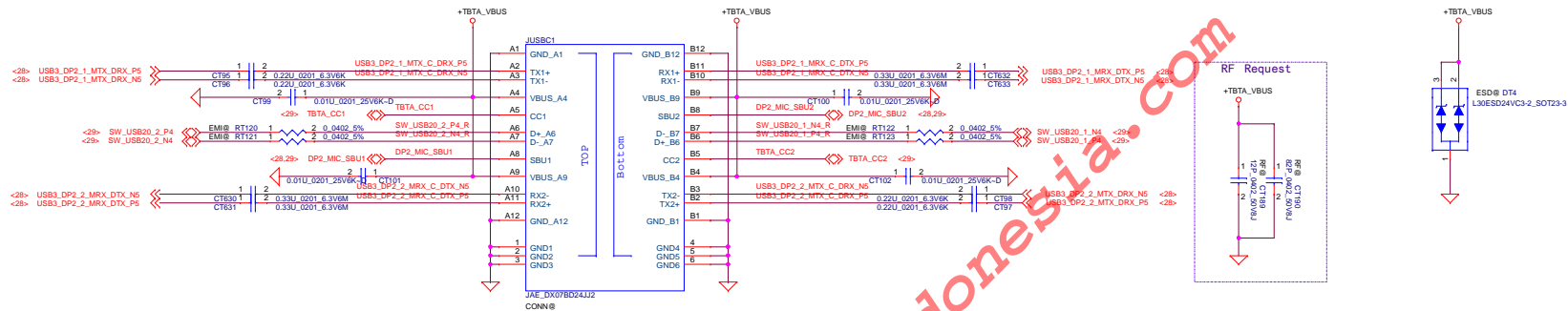
change TPS65982DB -> DC



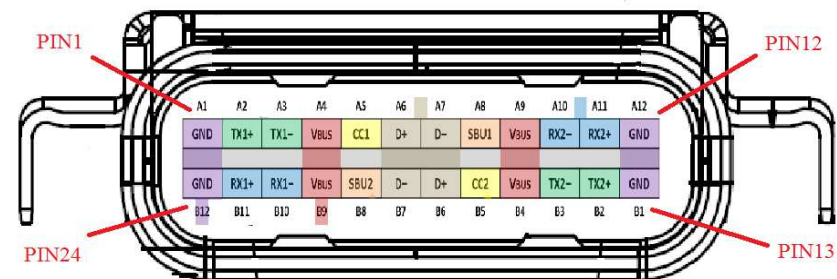
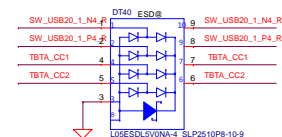
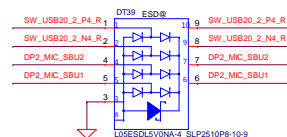
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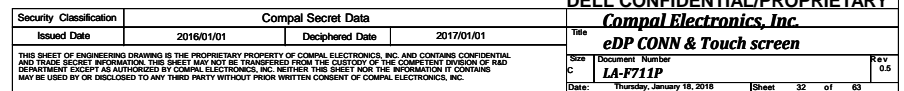
CT630~633 use SD043000080 (0 ohm) for CSLP3 build



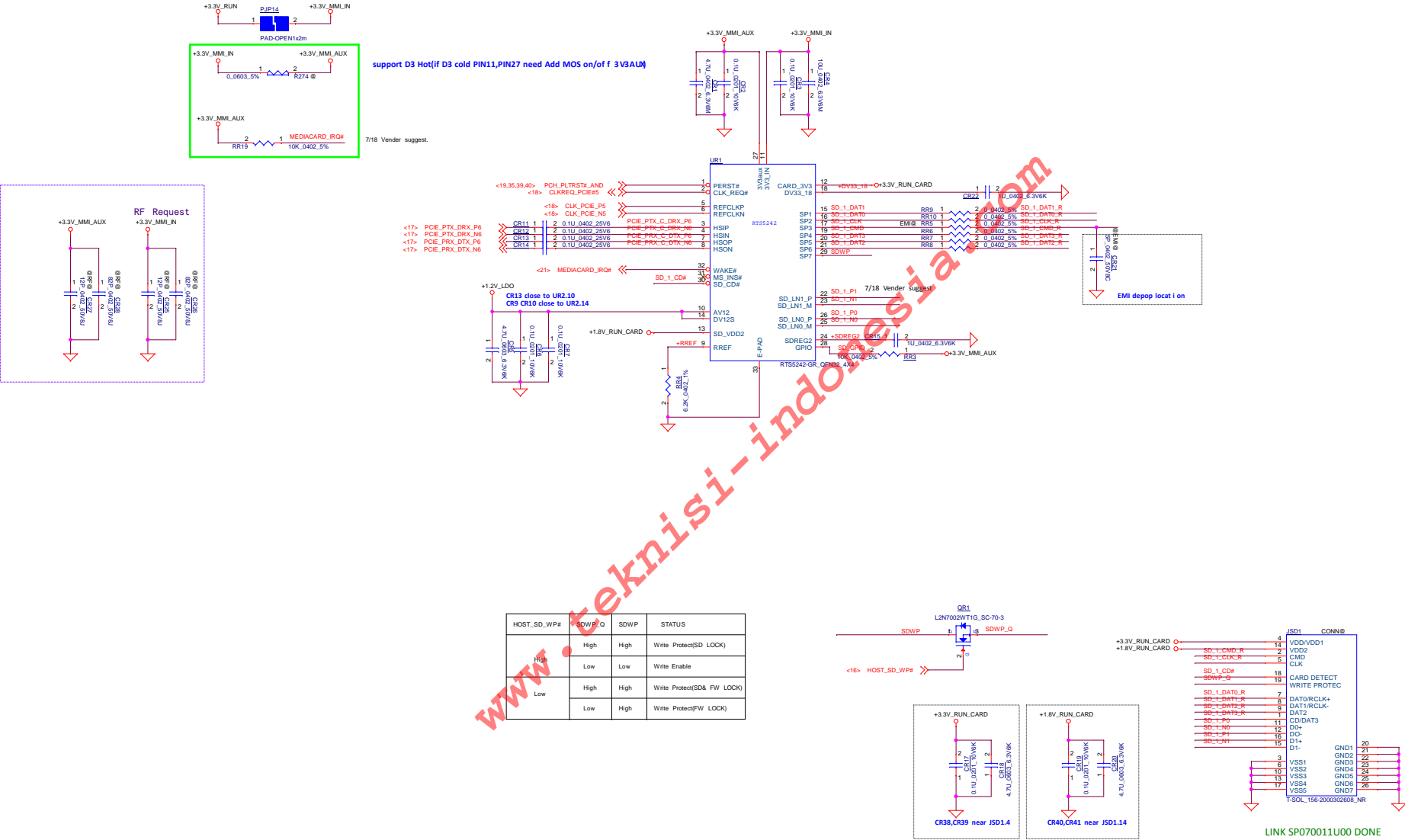
change typeC ESD part from SC40000AR00 to SC40000DF00

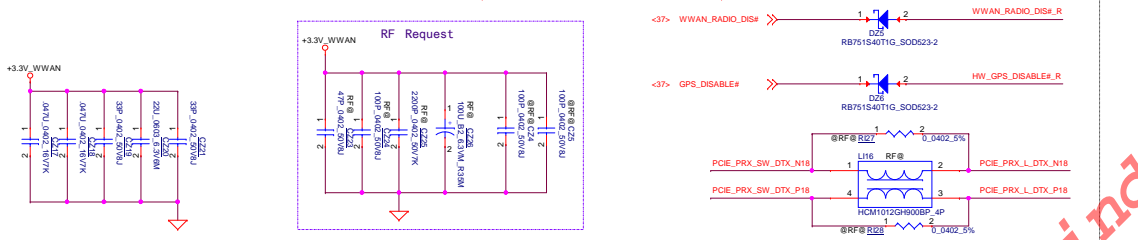
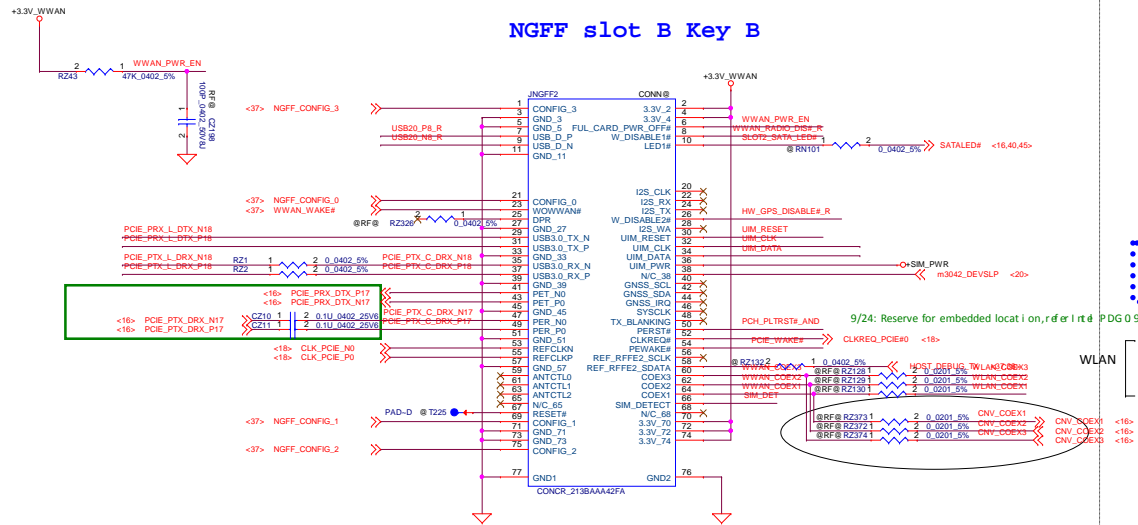


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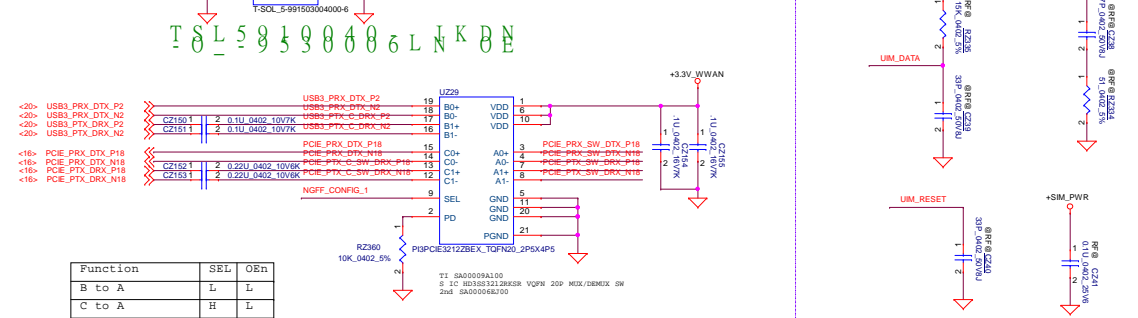
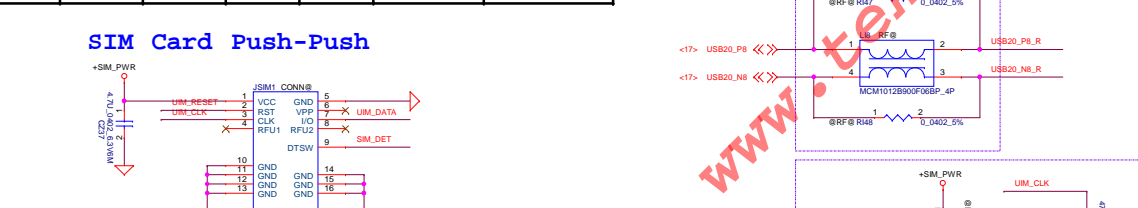


For PCIE Interface

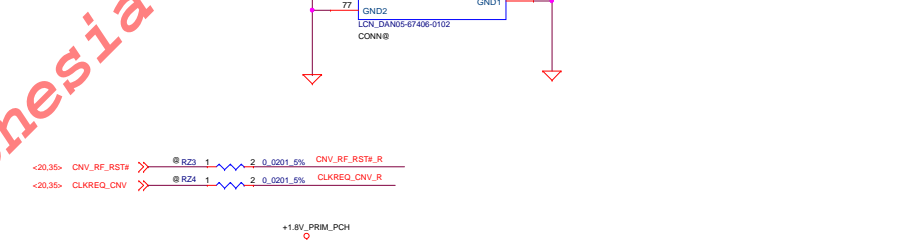
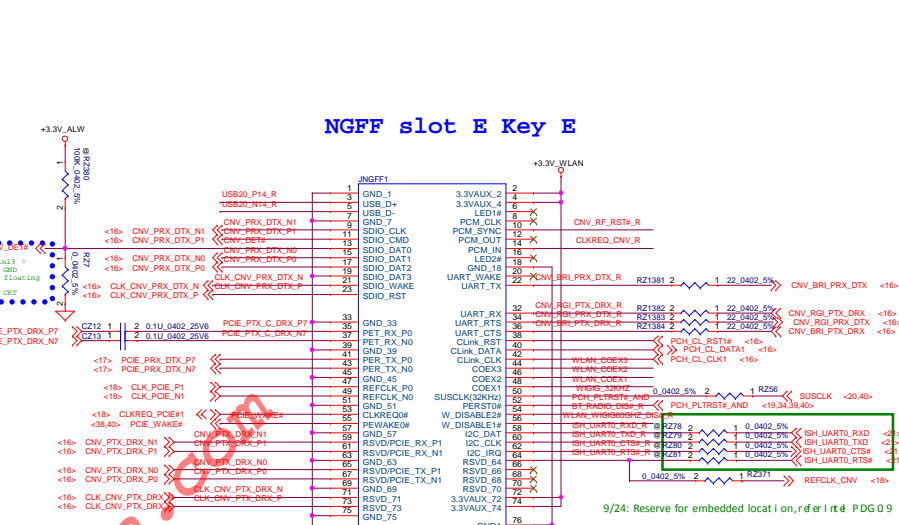




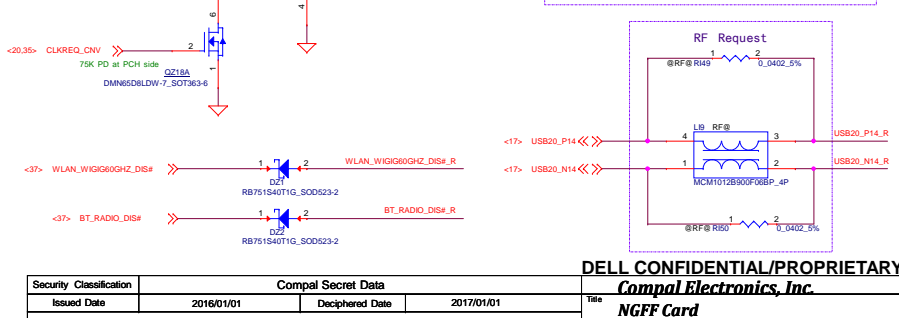
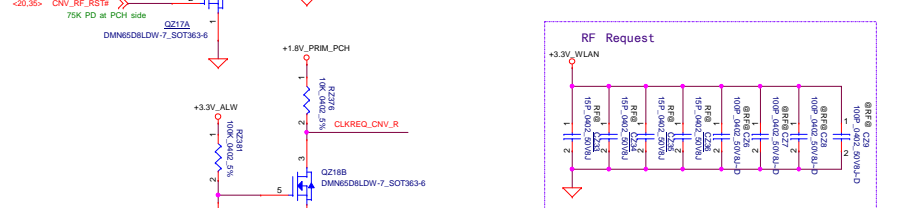
STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	m3042_PCIE#_SATA
0	GND	GND	GND	GND	SSD-SATA	High
1	GND	HIGH	GND	GND	SSD-PCIe(2 lane)	Low
8	HIGH	GND	GND	GND	WWAN	Low
14	HIGH	GND	HIGH	HIGH	HCA-PCIe(1 lane)	Low
15	HIGH	HIGH	HIGH	HIGH	NA	Low



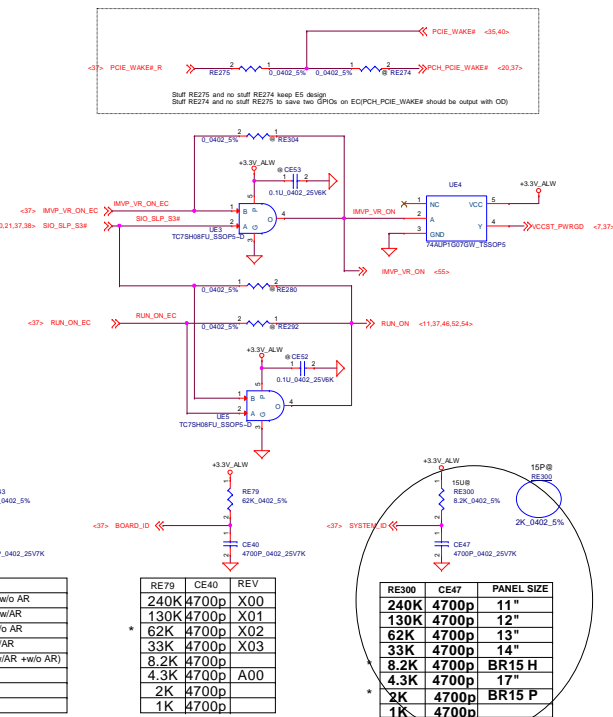
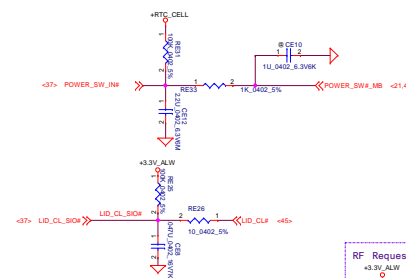
Function	SEL	OE#
B to A	L	L
C to A	H	L
All ports Hi-Z, IC power down	X	H



STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	m3042_PCIE#_SATA
0	GND	GND	GND	GND	SSD-SATA	High
1	GND	HIGH	GND	GND	SSD-PCIe(2 lane)	Low
8	HIGH	GND	GND	GND	WWAN	Low
14	HIGH	GND	HIGH	HIGH	HCA-PCIe(1 lane)	Low
15	HIGH	HIGH	HIGH	HIGH	NA	Low



Function	SEL	OE#
B to A	L	L
C to A	H	L
All ports Hi-Z, IC power down	X	H



	RE343	CE62	REV
*	240K	4700p	Single Port ACE w/o AR
	130K	4700p	Single Port ACE w/AR
	62K	4700p	Dual Port ACE w/o AR
	33K	4700p	Dual Port ACE w/AR
	8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
	4.3K	4700p	.
	2K	4700p	
	1K	4700p	

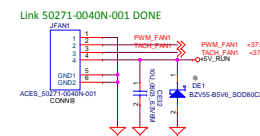
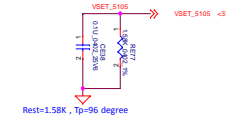
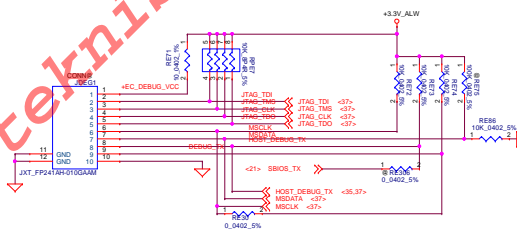
RE79	CE40	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	
4.3K	4700p	A00
2K	4700p	
1K	4700p	

RE300	CE47	PANEL SIZE
240K	4700p	11"
130K	4700p	12"
62K	4700p	13"
33K	4700p	14"
8.2K	4700p	BR15 H
4.3K	4700p	17"
2K	4700p	BR15 P
1K	4700p	

PD_ACE_DET# rise times measured from 5% 68

BOARD_ID rise times measured from 5%~68%

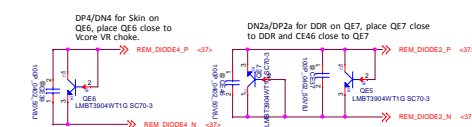
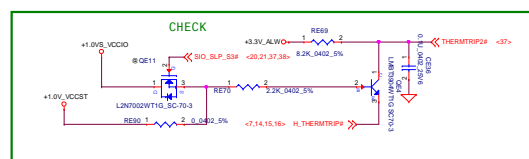
PANEL_ID rise t i n e i s m e a s u r e d f r o m 5 % - 6 8 %

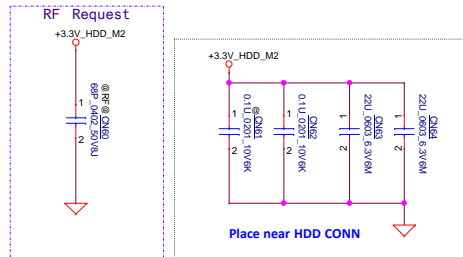


Thermal diode mapping	
5105 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	WiGig (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)

Place under CPU
Place CE35 close to the QE3 as possible

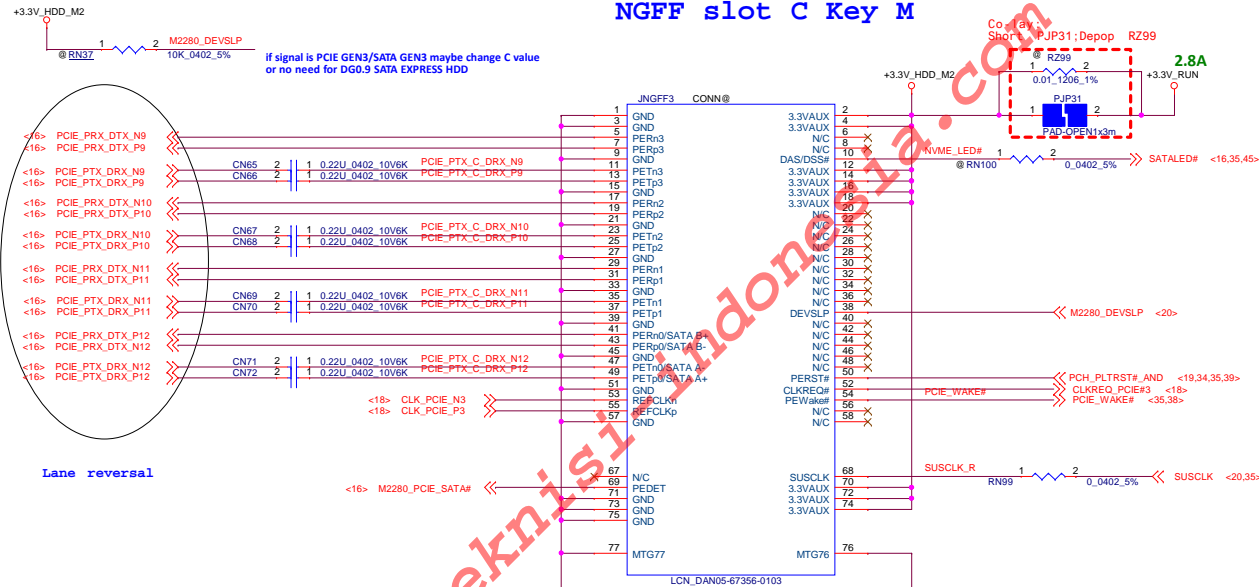
DP2/DN2 for WiGig on QE5, place QE5 close to Type-C and CE37 close to QE5





2280 SSD

NGFF slot C Key M

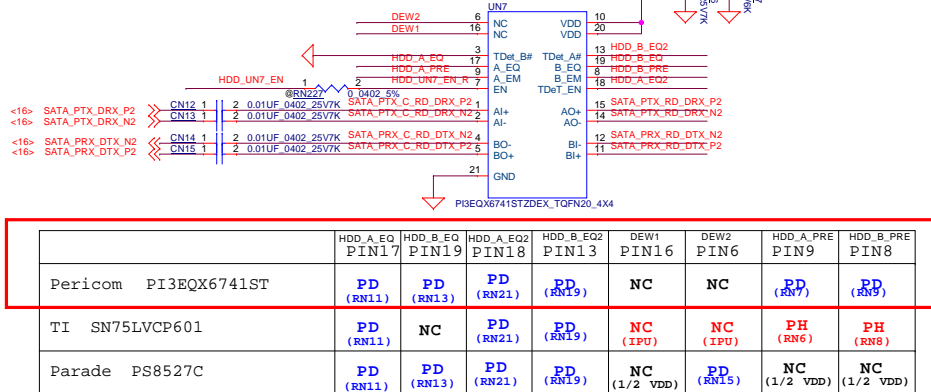


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				M2 2280 Socket	
Size	Document Number			Rev	
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	pin.3	pin.6	pin.13	pin.16	pin.18
Peric	TDet_#	N	TDet_A#	N	TDet_EN
TDet_#	N	TDet_A#	N	TDet_EN	
TDet_A#	N	TDet_EN			
TDet_EN					

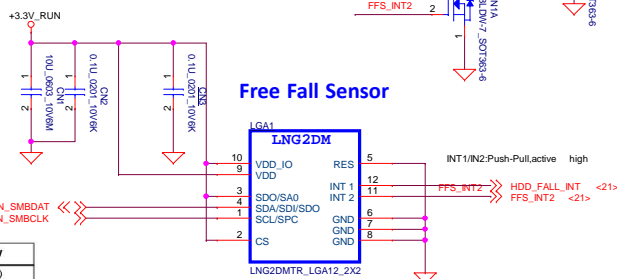
SATA Repeater



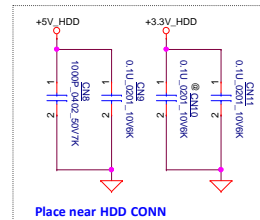
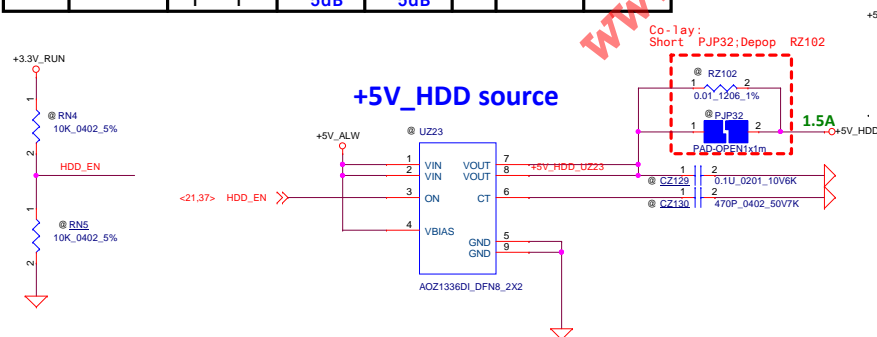
			A_EQ	B_EQ		A_EM	B_EM
Main	Pericom	0	3dB	3dB	0	0dB	0dB
		1	6dB	6dB	1	1.5dB	1.5dB
			9dB	9dB			
2nd	TI	0	7dB	7dB	0	0dB	0dB
		1	0dB	0dB	1	-4dB	-4dB
			14dB	14dB		-2dB	-2dB
3rd	Parade	EQ2	A_EQ	B_EQ		A_EM	B_EM
		(M = VDD/2)					
		0	2.4dB	2.4dB	0	0dB	0dB
		0	7.4dB	7.4dB	0	0dB	0dB
		0	14.4dB	14.4dB	0	0dB	0dB
		0	12.2dB	12.2dB	0	0dB	0dB
		0	9.4dB	9.4dB	0	0dB	0dB
		0	13.3dB	13.3dB	0	0dB	0dB
		0	6.2dB	6.2dB	0	0dB	0dB
		0	11.2dB	11.2dB	0	0dB	0dB
		0	5dB	5dB	0	0dB	0dB

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)

Free Fall Sensor



+5V_HDD source



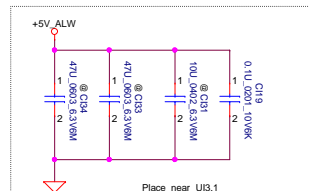
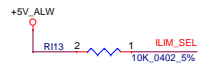
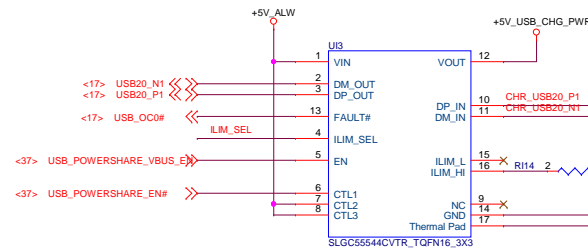
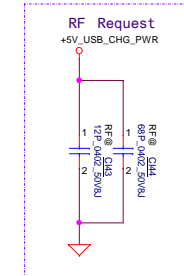
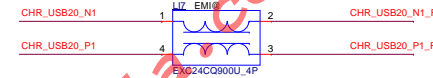
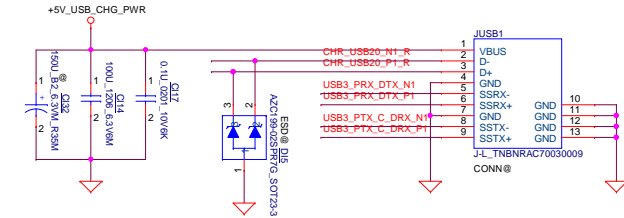
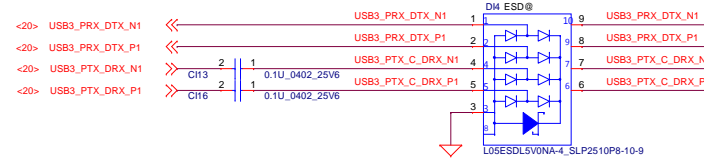
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Size	Document Number
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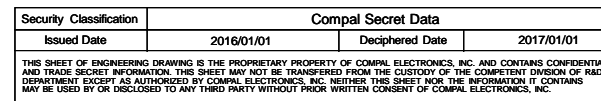
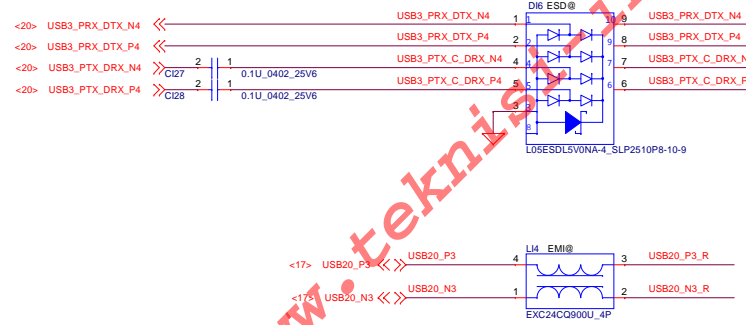
For PWR SW + Charger combine IC



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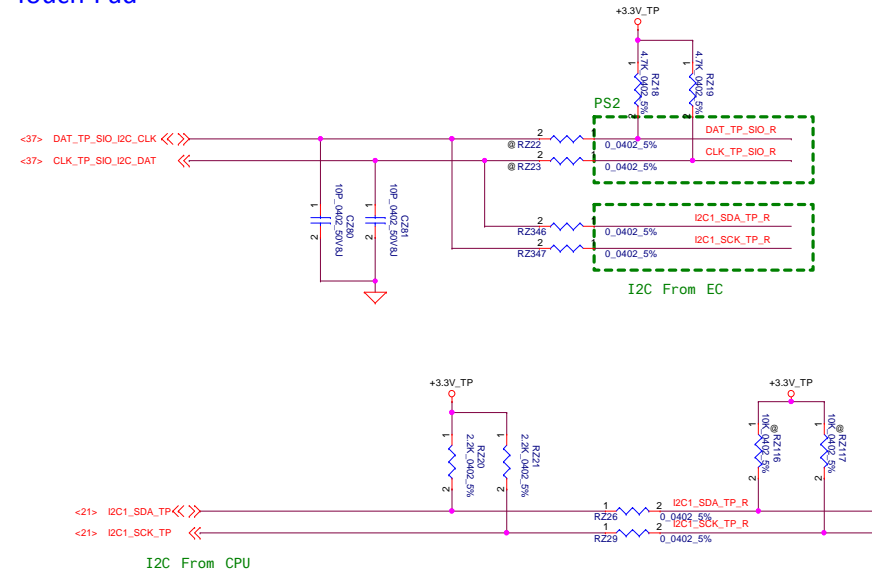
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The diagram shows the USB3.0 signal traces and components. The top section shows the USB3.0 signal traces (USB3_PRX_DTX_N4, USB3_PRX_DTX_P4, USB3_PTX_C_DRX_N4, USB3_PTX_C_DRX_P4) connected to the L05ESDL5V0N4-SLP2510P8-10-9 component. The bottom section shows the USB2.0 signal traces (USB20_P3, USB20_N3) connected to the EXC24CQ900U_4P component. A detailed view of the USB3.0 signal traces shows the RF Request signal (RF@_CH7) and the USB3_EX3_PWR signal. The RF Request signal is connected to the RF@_CH7 pin of the L05ESDL5V0N4-SLP2510P8-10-9 component. The USB3_EX3_PWR signal is connected to the USB3_EX3_PWR pin of the L05ESDL5V0N4-SLP2510P8-10-9 component. The USB2.0 signal traces are connected to the EXC24CQ900U_4P component. The EXC24CQ900U_4P component is connected to the USB20_P3 and USB20_N3 signal traces. The EXC24CQ900U_4P component is also connected to the +5V_ALW signal trace. The EXC24CQ900U_4P component is connected to the GND signal trace. The EXC24CQ900U_4P component is connected to the USB20_P3 and USB20_N3 signal traces. The EXC24CQ900U_4P component is connected to the +5V_ALW signal trace. The EXC24CQ900U_4P component is connected to the GND signal trace.

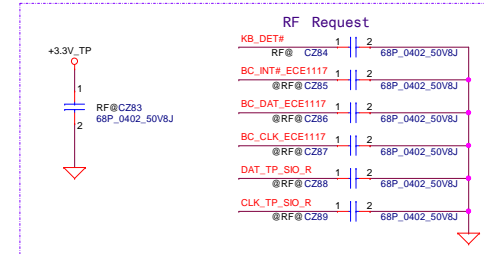
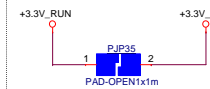


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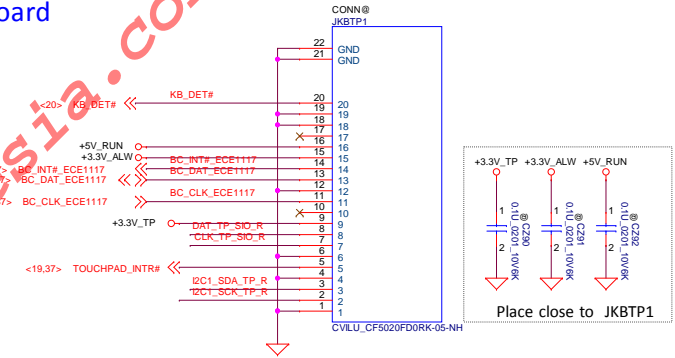
Touch Pad



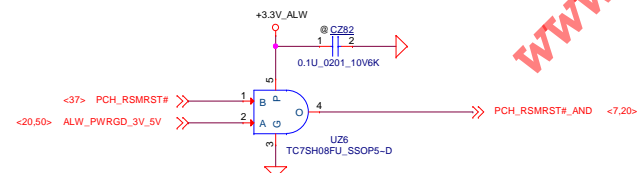
Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7)
For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows
Route PS2 from EC to the touch pad also for contingency plan if I2C has issues



Keyboard



RSMRST circuit



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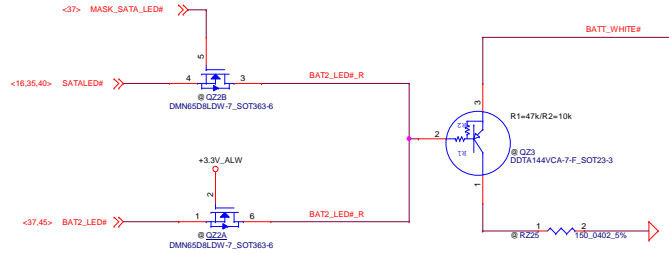
Compal Electronics, Inc.

Keyboard

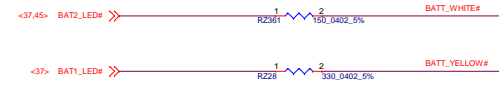
LA-F711P

HDD LED MUX

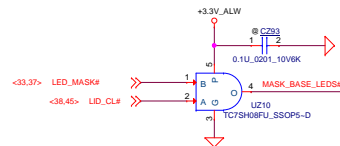
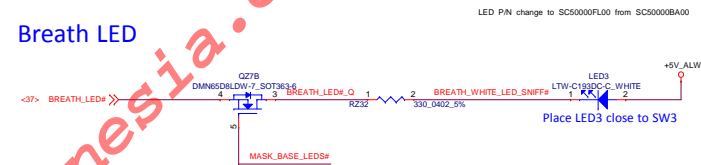
means EC can switch battery white led and HDD LED by hot key ~ Fn+H



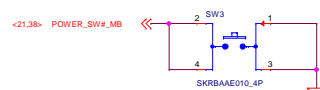
Battery LED



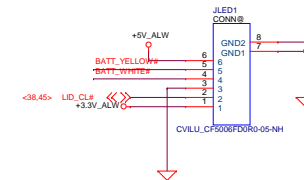
Breath LED



POWER & INSTANT ON SWITCH



LED board CONN

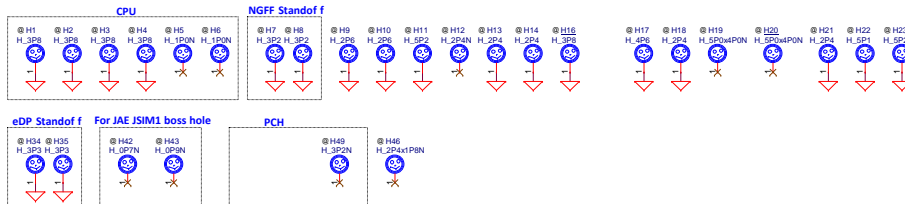


Fiducial Mark



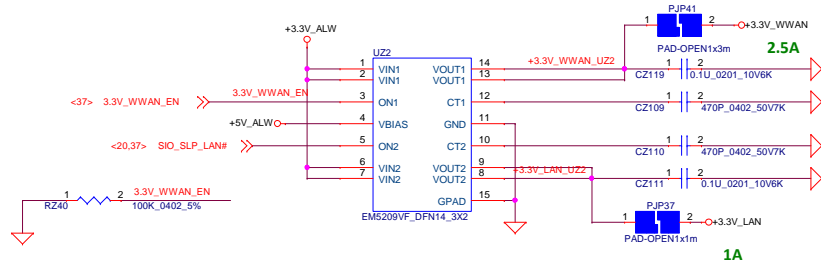
LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not mask LEDs (Lid Opened)	1	1



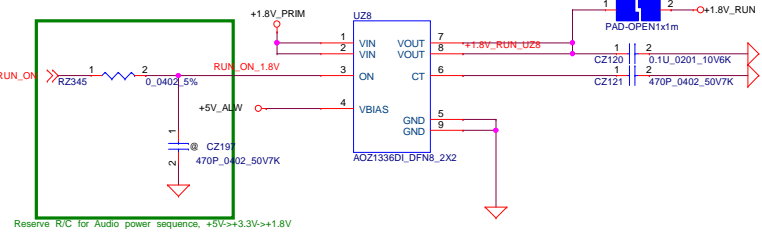
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Title			Compal Electronics, Inc.
Document Number			PAD, LED
Rev			05
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+3.3V_WWAN/+3.3V_LAN source



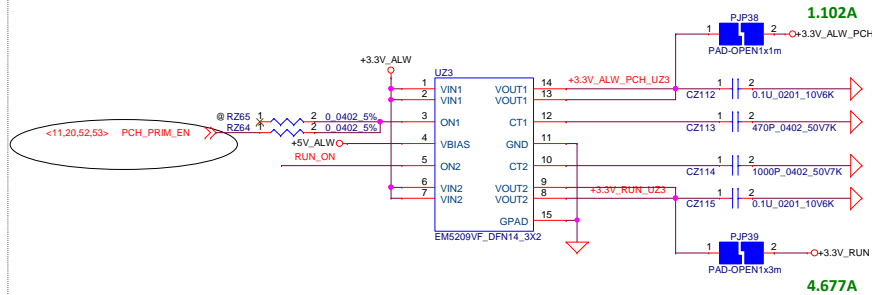
1A

+1.8V_RUN source



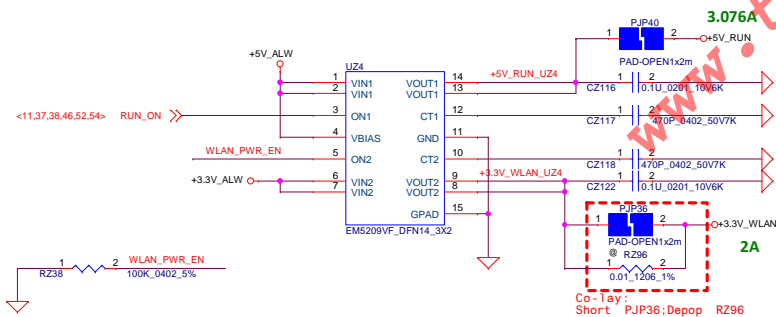
0.025A

+3.3V_ALW_PCH/+3.3V_RUN source



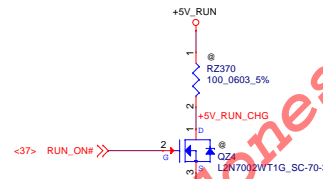
4.677A

+5V_RUN/+3.3V_WLAN source

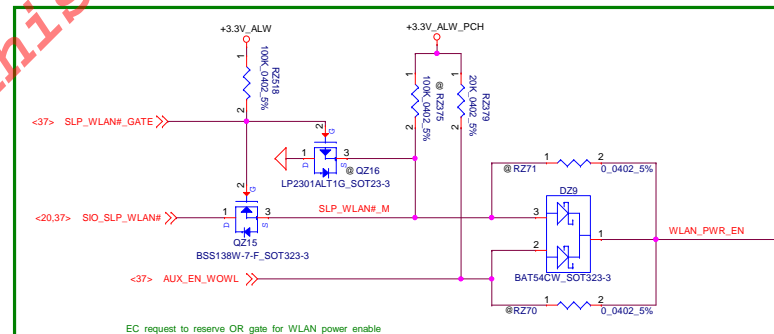


2A

Co-Lay:
Short PJP36;Depop RZ96

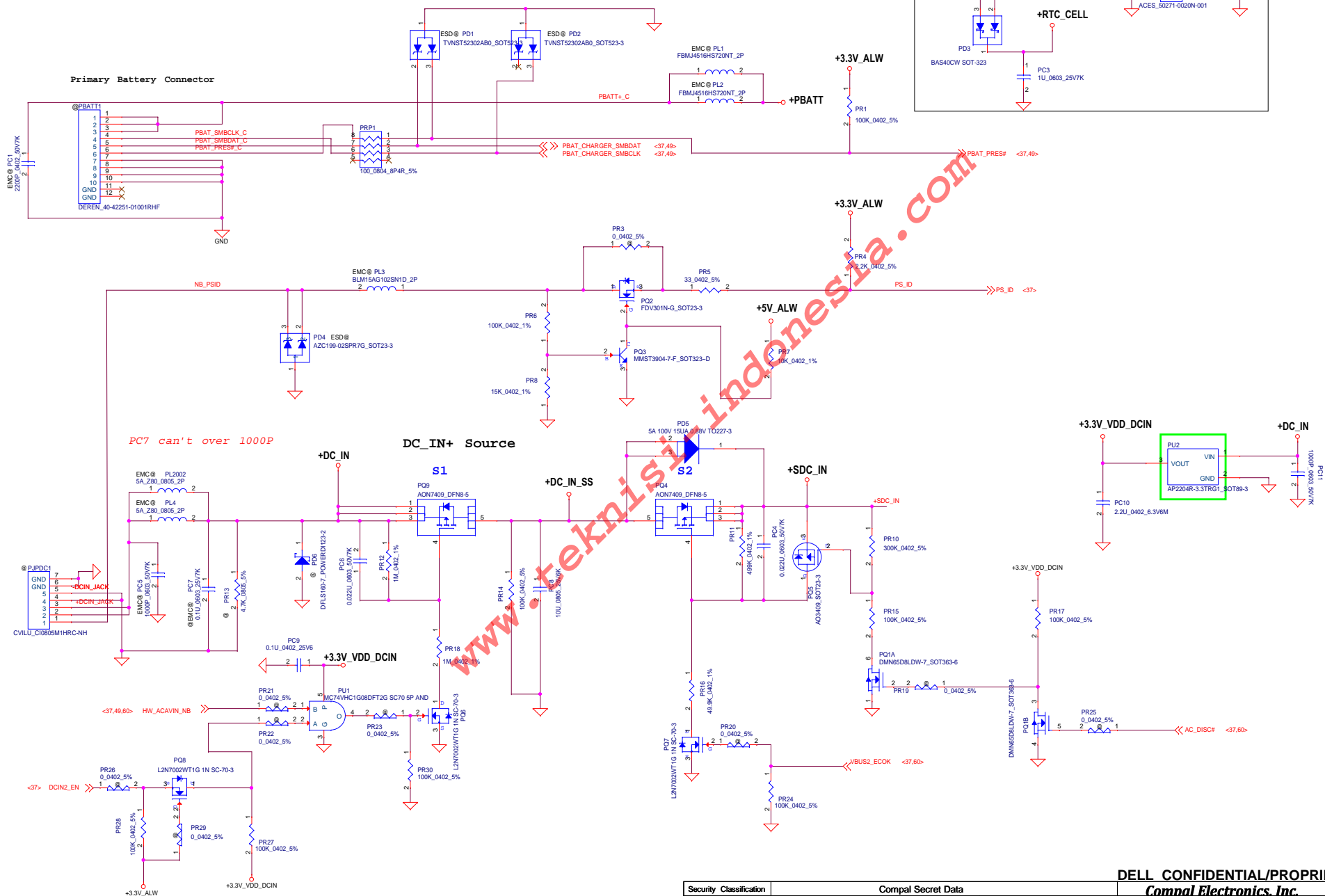


Reserve for S3 no power issue (+5V_RUN discharge circuit)

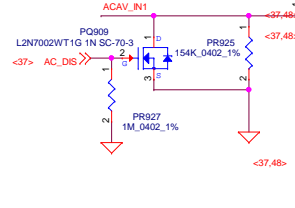
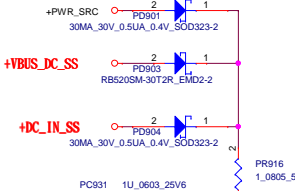
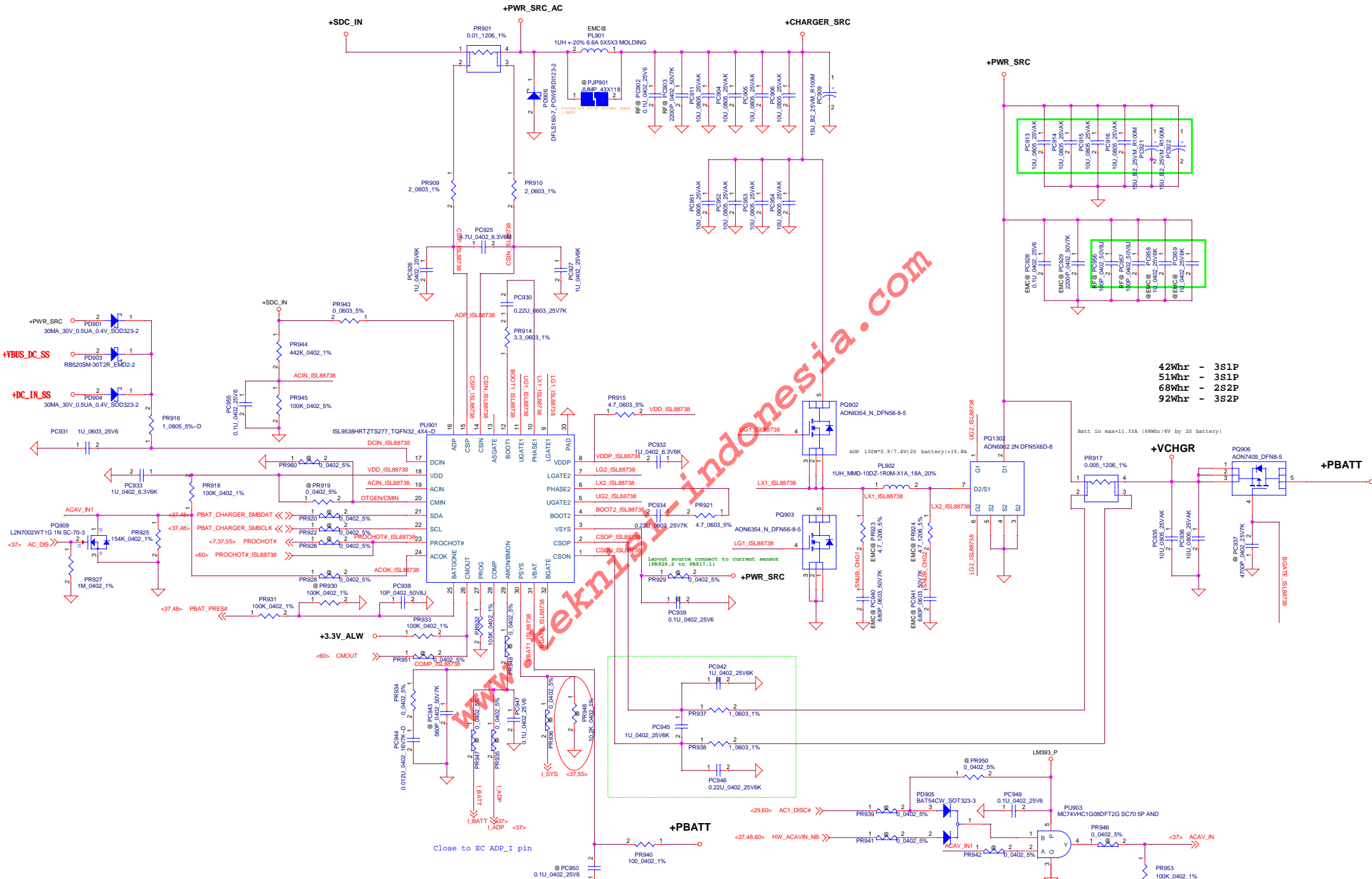


EC request to reserve OR gate for WLAN power enable

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								LA-F711P			
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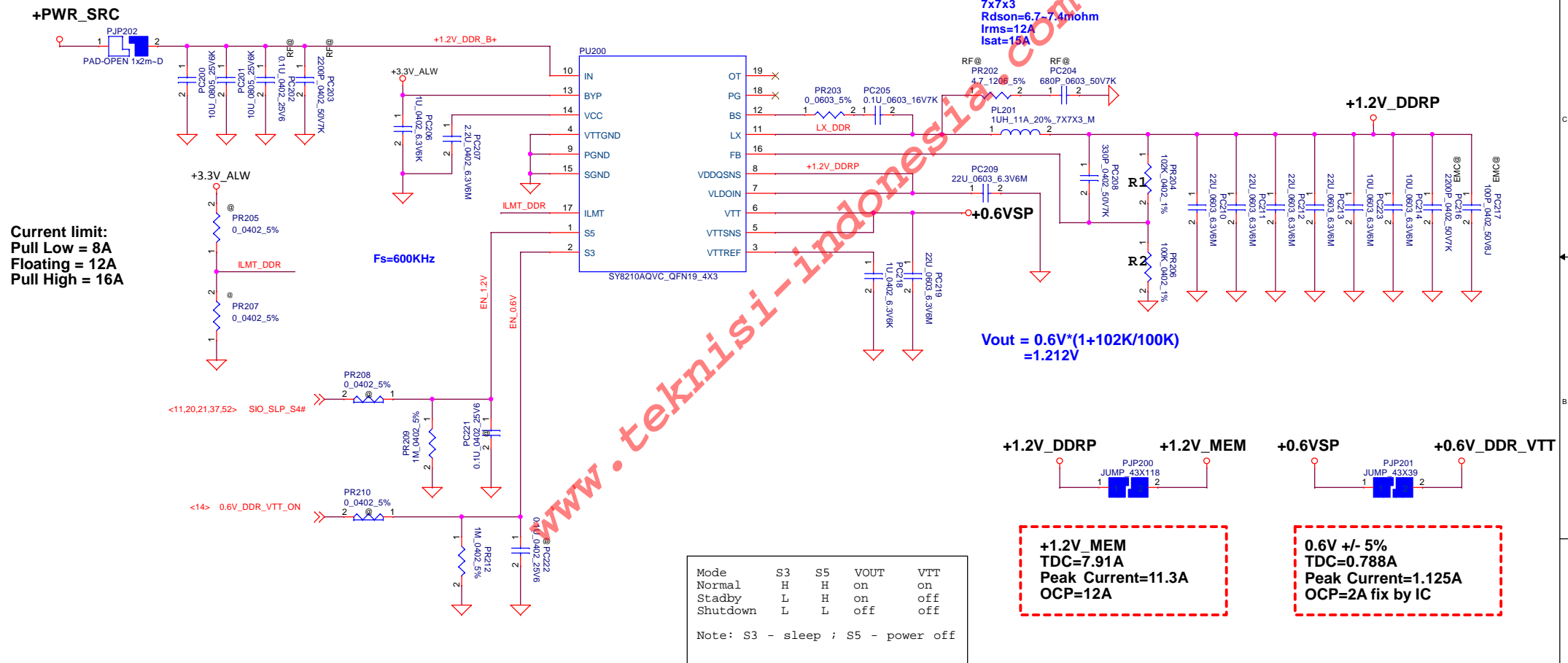
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2017/01/01		2018/01/01		+DCIN	
Size		Document Number		Rev	
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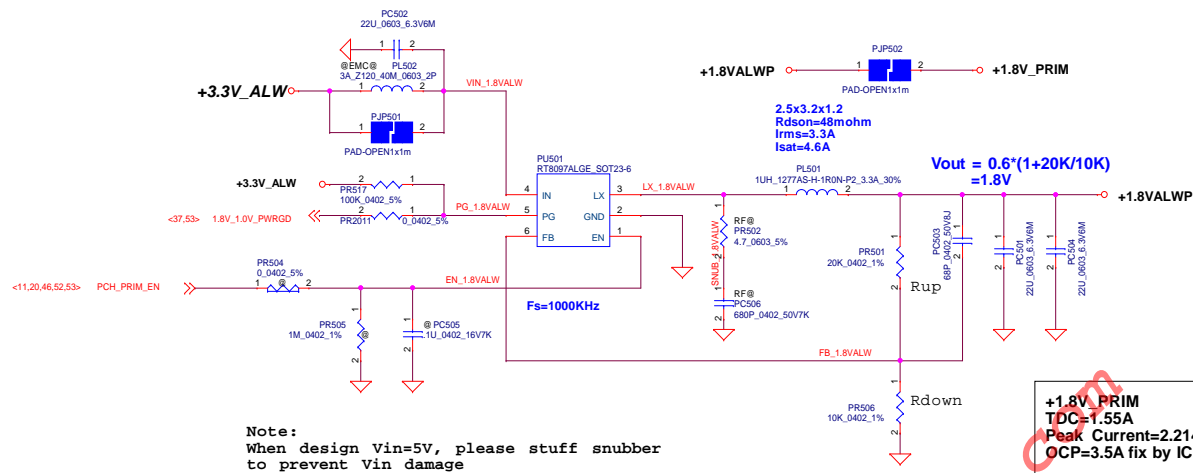


Adp=130W, Battery Max=12.9V*9.7A=125.13W
 Psys_max = 255.13W, Set PSYS=225W
 Ipsys = (1.493/2) * Psys_max + 1.43 = 169.39uA
 Rpsys = 2 / Ipsys=11.8kOhm
 Place at CPU_VR side

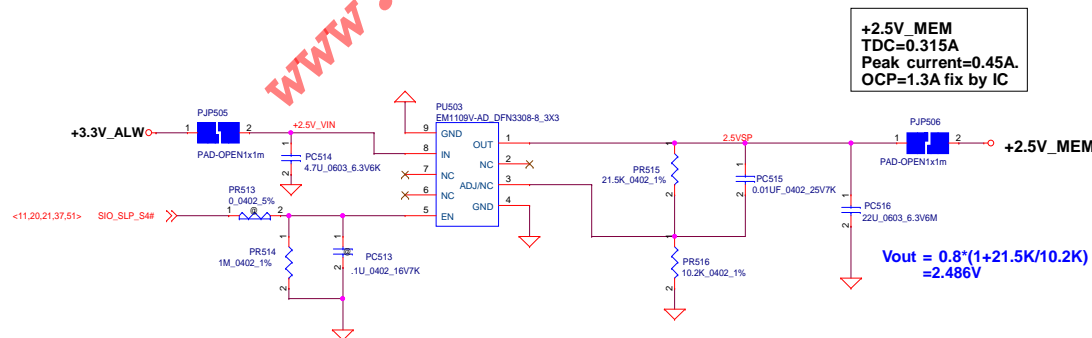
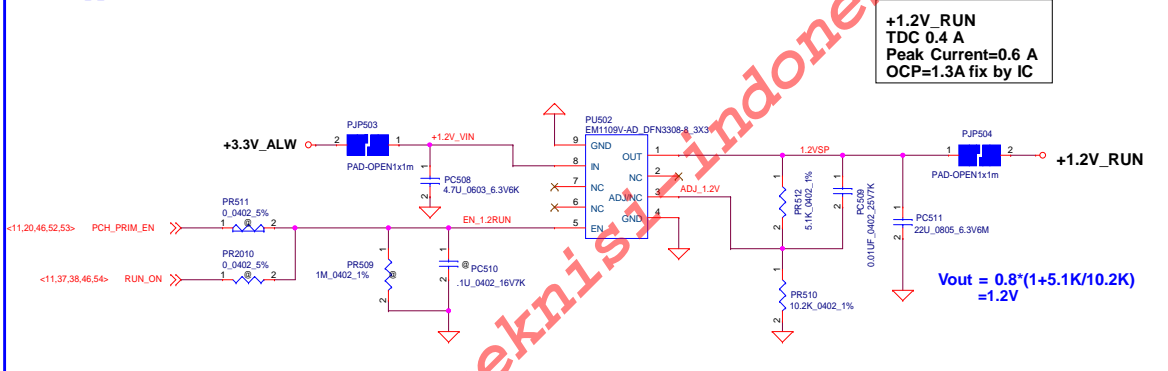
42Whr - 3S1P
 51Whr - 3S1P
 68Whr - 2S2P
 92Whr - 3S2P

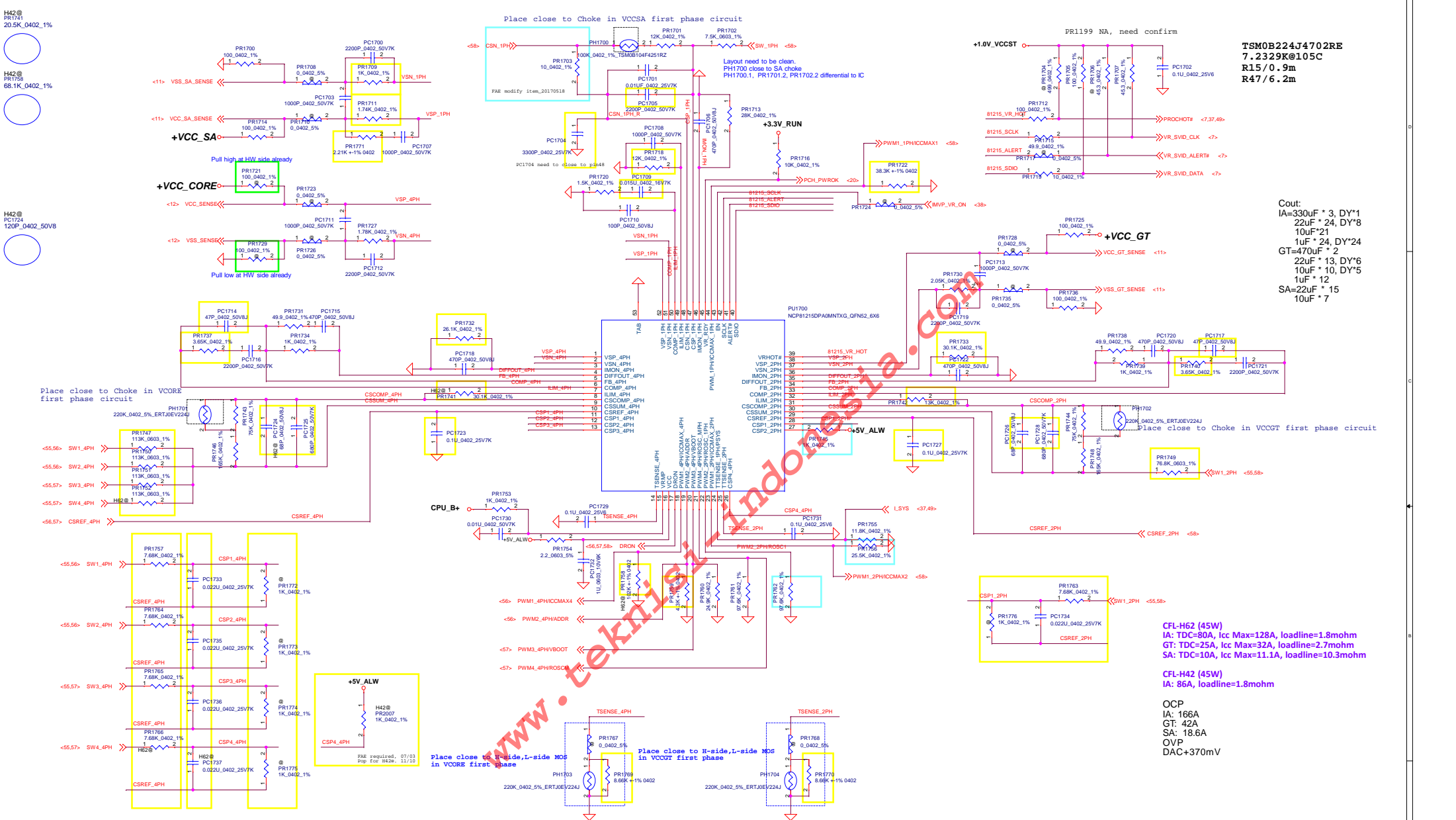
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For TypeC-SW PS8802





TSM0B224J4702RE
7.2329K@105C
R15/0.9m
R47/6.2m

Cout:
IA=330uF * 3, DY*1
22uF * 24, DY*8
10uF * 21
1uF * 24, DY*24
GT=470uF * 2
22uF * 13, DY*6
10uF * 10, DY*5
1uF * 12
SA=22uF * 15
10uF * 7

CFL-H62 (45W)
IA: TDC=80A, Icc Max=128A, loadline=1.8mohm
GT: TDC=25A, Icc Max=32A, loadline=2.7mohm
SA: TDC=10A, Icc Max=11.1A, loadline=10.3mohm

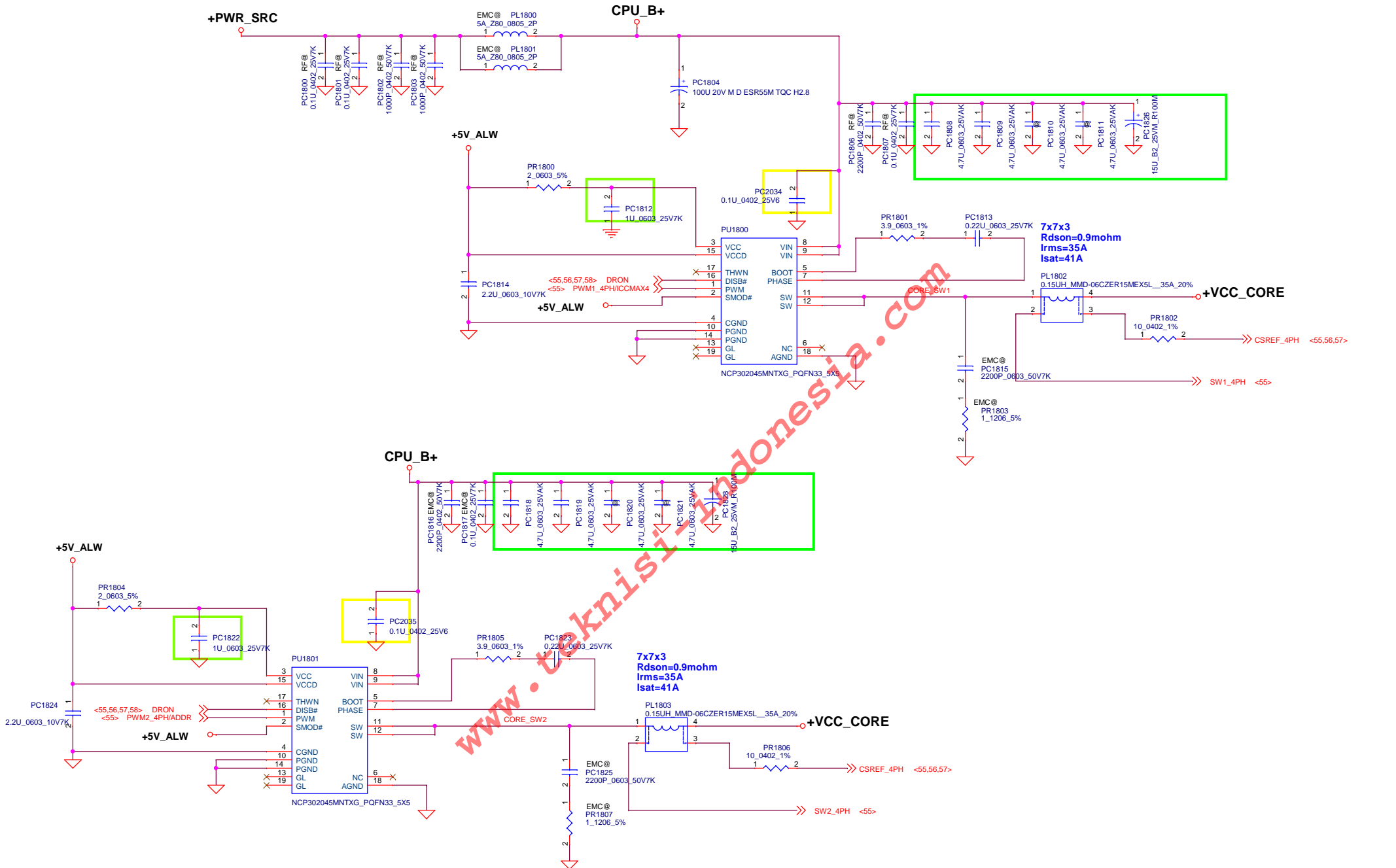
CFL-H42 (45W)
IA: 86A, loadline=1.8mohm

OCF
IA: 166A
GT: 42A
SA: 18.6A
OVP
DAC+370mV

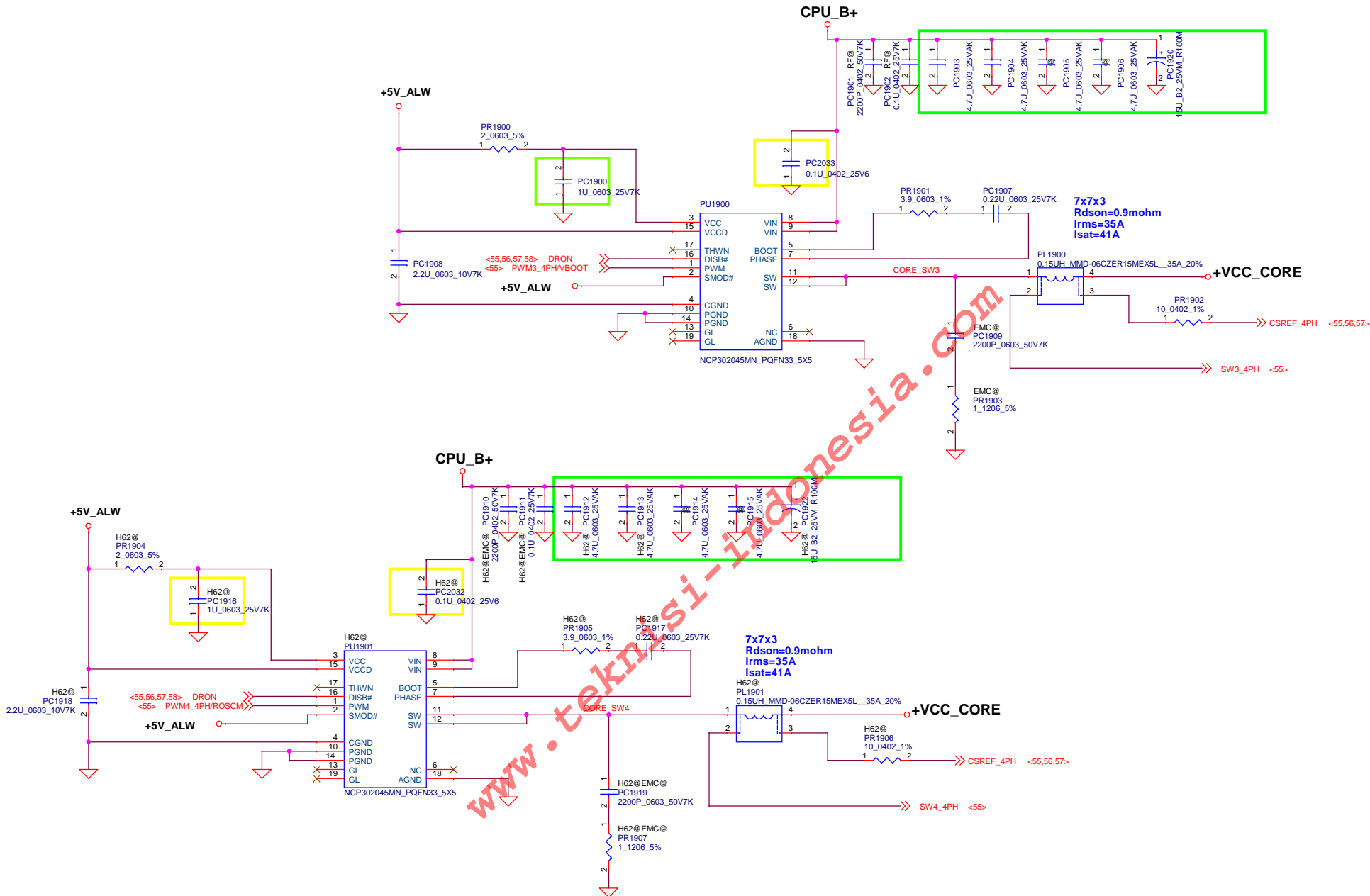
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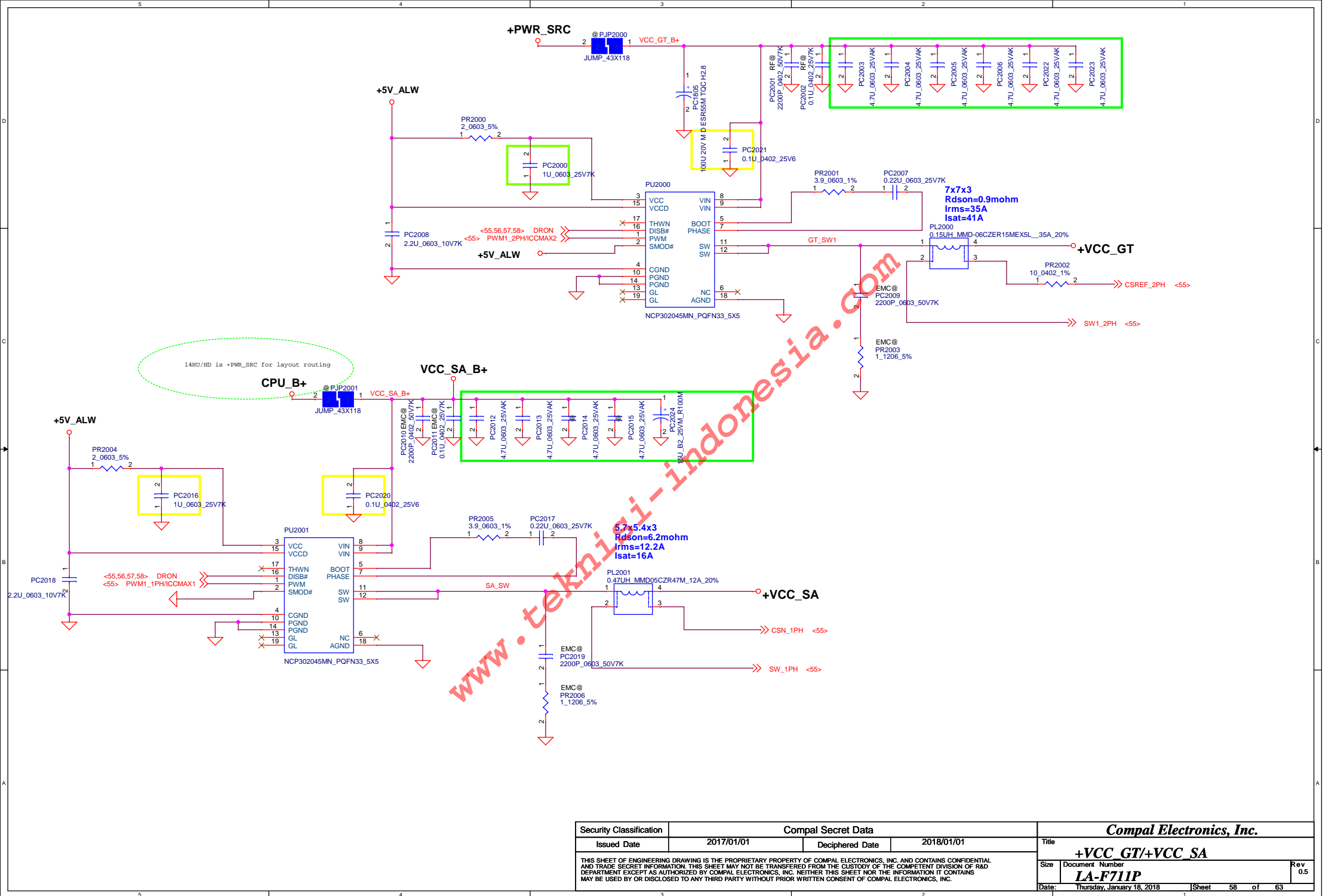
Compal Electronics, Inc.	
NCP81215	
LA-F711P	
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VCC_CORE Place on CPU
Back Side.
22U_0603 * 13 pcs + 10U_0402*21 pcs + 1U_0201*24 pcs
Primary Side.
22U_0603 * 11 pcs+330u_D2*3 pcs

+VCC_CORE

Follow Intel

Cout:
IA=330uF * 3, DY*1
22uF * 24, DY*8
10uF*21
1uF * 24, DY*24
GT=470uF * 2
22uF * 13, DY*6
10uF * 10, DY*5
1uF * 12
SA=22uF * 15
10uF * 7

VCC_GT Place on CPU

Back Side.
22U_0603 * 6 pcs +10U_0402*10 pcs +1U_0201*12 pcs
Primary Side.
22U_0603 * 7 pcs +470u_D2*2 pcs

+VCC_GT

+VCC_SA

Reduce SA acoustic

VCC_SA Place on CPU

Back Side.
22U_0603 * 10 pcs + 10U_0402*7 pcs
Primary Side.
22U_0603 * 5pcs

+VCC_CORE

+VCC_CORE Place on CPU
1U_0201*24 pcs (placeholder)

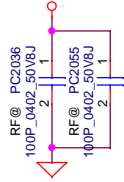
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Issued Date	2017/01/01	Deciphered Date	2018/01/01
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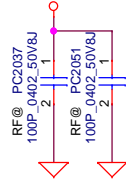
Compal Electronics, Inc.
PROCESSOR DECOUPLING

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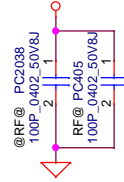
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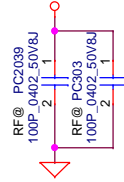
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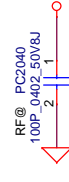
VIN_1VS_VCCIO



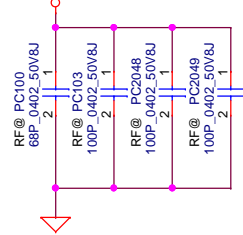
+1VALWP_B+



+3.3V_ALWP



3V_VIN



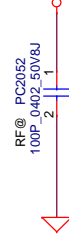
5V_VIN



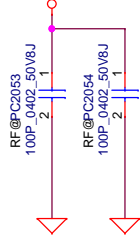
+1.2V_DDRP



VCC_SA_B+



CPU_B+



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Version Change List (P. I. R. List)

Item	Date	Reason for change	Description	Phase
1	2017/11/17	Follow Intel design Fine tune PSYS setting to 225W Fine tune PCH sequence	Unpop PC1052 Unpop PR948, change PR1755 to 11.8K ohm Change PR312 to 15K ohm	X02
2	2017/11/17	Update CPU VR circuit to support H42 CPU	Change PC1705 to 2.2nF, PC1726 to 68pF, PR1749 to 76.8K, PR1730 to 2.05K, PR1727 to 1.78K, Change PC1724 to 68pF for H62 Unpop PR1752, PR1766, PC1737, PC1910, PC1911, PC1912, PC1913, PC1916, PC1917, PC1918, PC1919, PC1922, PC2032, PL1901, PR1904, PR1905, PR1906, PR1907, PU1901 Pop PR2007 1K ohm	X02
3	2017/12/08	For RF requirement	Add PC2053, PC2054, PC2055	X02
4	2018/01/04	Reserve for power on sequence modified	Add PR2010 0ohm, Reserve PR2011, PR2012, modify 1.8V_PRIM_PWRGD to 1.8V_1.0V_PWRGD	X02
5	2018/01/08	Change 0ohm to Short PAD Change JUMP to NPM footprint	Change PR26, PR29, PR21, PR22, PR23, PR20, PR19, PR25, PR960, PR920, PR922, PR926, PR928, PR951, PR947, PR935, PR936, PR929, PR939, PR941, PR942, PR946, PR949, PR104, PR105, PR119, PR120, PR114, PR208, PR210, PR504, PR511, PR513, PR314, PR315, PR402, PR414, PR1708, PR1710, PR1723, PR1726, PR1767, PR1768, PR1728, PR1735, PR1724, PR1717, PR1238, PR1250, PR1211, PR1215, PR1216, PR1220, PR1218, PR1223, PR1242, PR1257, PR1244, PR1241, PR1245 to short PAD Change PJP901 to JUMP_43X118-NPM	X02

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				PWR P.I.R	
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				Drawn: LA-F711P	01
				Check: Thursday, January 18, 2019	01

Version Change List (P. I. R. List)								
Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.	
1		all	HW	2017/08/22	COMPAL	1. Add soft start solution(only reserved) on QV8,QE1 (add CV143H, C21200, R21380,RV1400) 2. Add soft start solution(only reserved) on QE15,QH7 (add CE140,RE145) 3. reserve RV9, CV143H	0.2(X01)	
					To avoid in-rush current caused voltage drop			
2		4	HW	2017/08/22	COMPAL	depop RC324	0.2 (X01)	
3		37	HW	2017/08/22	COMPAL	board ID	0.2 (X01)	
4		35	HW	2017/08/22	COMPAL	modify CLKREQ_CNV & detect pin circuit	0.2 (X01)	
5		21	HW	2017/08/22	COMPAL	TPM pin connectivity requirement	0.2 (X01)	
6		11	HW	2017/08/22	COMPAL	External Power data control for C10.	0.2 (X01)	
7		35	HW	2017/08/22	COMPAL	Intel PDG rev. 1.0 updated	0.2 (X01)	
8		37	HW	2017/08/22	COMPAL	GPIO map for EC	0.2 (X01)	
9		41	HW	2017/08/22	COMPAL	DELL sch. review	0.2 (X01)	
10		37	HW	2017/08/22	COMPAL	To avoid USB_POWERSTATE spike before EC stable when power up.(follow WH)	0.2 (X01)	
11		27	HW	2017/08/22	COMPAL	VDR BA request	0.2 (X01)	
12		all	HW	2017/08/22	COMPAL	Xial BA request	0.2 (X01)	
13		all	HW	2017/08/22	COMPAL	RF request	0.2 (X01)	
14		adp	HW	2017/09/20	COMPAL	touch screen, soft start reserve	0.2 (X01)	
15		audio	HW	2017/09/20	COMPAL	audio BA request	0.2 (X01)	
16		typeC SW	HW	2017/09/20	COMPAL	typeC BA request	0.2 (X01)	
17		EC	HW	2017/09/20	COMPAL	vendor request	0.2 (X01)	
18		adp	HW	2017/12/13	COMPAL	battery life request	0.3 (X01)	
19		CPUPCH	HW	2017/12/13	COMPAL	Intel guideline update	0.3 (X01)	
20		EC	HW	2017/12/13	COMPAL	follow EC request for R10	0.3 (X01)	
21		adp	HW	2017/12/13	COMPAL	DELL request	0.3 (X01)	
22		cpu	HW	2017/12/13	COMPAL	SDP request	0.3 (X01)	
23		cpu	HW	2017/12/13	COMPAL	add short protection fot typeC	0.3 (X01)	
24		CHV1	HW	2017/12/13	COMPAL	intel H0W50 CHV1 Wp update	0.3 (X01)	
25		EC	HW	2017/12/13	COMPAL	board ID	0.3 (X01)	
26		TPM	HW	2018/01/08	COMPAL	TPM change to WP part	0.4 (X02)	
27		EC	HW	2018/01/08	COMPAL	reserve for power on sequence modification	0.4 (X02)	
28		cpu	HW	2018/01/08	COMPAL	Intel PDG updated	0.4 (X02)	
29		typeC SW	HW	2018/01/08	COMPAL	USB3.1 Gen2 BA fail	0.5 (X02)	

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